

2022-1612

UNITED STATES COURT OF APPEALS FOR THE FEDERAL CIRCUIT

ANALOG DEVICES, INC.,

Appellant,

v.

XILINX, INC., XILINX ASIA PACIFIC PTE. LTD.,

Appellees.

**Appeal from the United States Patent and Trademark Office,
Patent Trial and Appeal Board in No. IPR2020-01561**

APPELLANT'S PRINCIPAL BRIEF

Janine A. Carlan
Taniel Anderson
Jasjit S. Vidwan
ArentFox Schiff LLP
1717 K Street, NW
Washington, DC 20006
202.857.6000
janine.carlan@afslaw.com

*Counsel for Appellant,
Analog Devices, Inc.*

Dated: November 3, 2022

U.S. Patent No. 7,719,452

Claims 1 and 13

Claim 1. An analog-to-digital converter system to convert an analog input signal to a system digital code, comprising:

 a sampler to provide samples of said analog input signal;

 signal converters arranged and configured to successively process said samples;

 at least one digital-to-analog converter configured to respond to a random digital code and inject analog dither signals into at least a selected one of said sampler and said signal converters which process said samples and said analog dither signals into a plurality of digital codes;

 an aligner/corrector coupled to said signal converters to process said plurality of digital codes into a combined digital code that includes a first portion that corresponds to said samples and a second portion that corresponds to said analog dither signals; and

 a decoder having a transfer function configured to convert said random digital code to said second portion for differencing with said combined digital code to thereby provide said system digital code;

 said samples thus processed along different signal-processing paths of said signal converters to thereby enhance linearity of said system.

Claim 13. An analog-to-digital converter system to convert an analog input signal to a system digital code, comprising:

signal converters arranged and configured to provide and successively process samples of said analog input signal;

at least one digital-to-analog converter configured to respond to a random digital code and inject corresponding analog dither signals into at least a selected one of said signal converters to enable said selected signal converter and succeeding signal converters to successively process said analog dither signals, processing of said samples and said analog dither signals thereby generating a plurality of digital codes;

an aligner/corrector coupled to said signal converters to process said plurality of digital codes into a combined digital code that includes a first portion that corresponds to said samples and a second portion that corresponds to said analog dither signals; and

a decoder having a transfer function configured to convert said random digital code to said second portion for differencing with said combined digital code to thereby provide said system digital code;

said samples thus processed along different signal-processing paths of said signal converters to thereby enhance conversion linearity of said system.

FORM 9. Certificate of Interest

Form 9 (p. 1)
July 2020

UNITED STATES COURT OF APPEALS
FOR THE FEDERAL CIRCUIT

CERTIFICATE OF INTEREST

Case Number 22-1612

Short Case Caption Analog Devices, Inc. v. Xilinx, Inc.

Filing Party/Entity Analog Devices, Inc.

Instructions: Complete each section of the form. In answering items 2 and 3, be specific as to which represented entities the answers apply; lack of specificity may result in non-compliance. **Please enter only one item per box; attach additional pages as needed and check the relevant box.** Counsel must immediately file an amended Certificate of Interest if information changes. Fed. Cir. R. 47.4(b).

I certify the following information and any attached sheets are accurate and complete to the best of my knowledge.

Date: 04/25/2022

Signature: /s/ Janine A. Carlan

Name: Janine A. Carlan

FORM 9. Certificate of Interest

Form 9 (p. 2)
July 2020

Additional pages attached

FORM 9. Certificate of Interest

Form 9 (p. 3)
July 2020

4. Legal Representatives. List all law firms, partners, and associates that (a) appeared for the entities in the originating court or agency or (b) are expected to appear in this court for the entities. Do not include those who have already entered an appearance in this court. Fed. Cir. R. 47.4(a)(4).

None/Not Applicable Additional pages attached

ArentFox Schiff LLP		

5. Related Cases. Provide the case titles and numbers of any case known to be pending in this court or any other court or agency that will directly affect or be directly affected by this court's decision in the pending appeal. Do not include the originating case number(s) for this case. Fed. Cir. R. 47.4(a)(5). See also Fed. Cir. R. 47.5(b).

None/Not Applicable Additional pages attached

Analog Devices, Inc. v. Xilinx, Inc. No. 1:19-cv-02225 (D. Del.)		

6. Organizational Victims and Bankruptcy Cases. Provide any information required under Fed. R. App. P. 26.1(b) (organizational victims in criminal cases) and 26.1(c) (bankruptcy case debtors and trustees). Fed. Cir. R. 47.4(a)(6).

None/Not Applicable Additional pages attached

2022-1612 Form 9. Certificate of Interest – Additional Page

Item 4. Legal Representatives.

A. Wilmer Cutler Pickering Hale and Dorr, LLP

- Peter Dichiara
- Cynthia D. Vreeland
- Scott Bertulli
- Jason Kipnis

B. Analog Devices, Inc.

- Michael Diener
- Claire Rollor
- Mihai Murgulescu

TABLE OF CONTENTS

STATEMENT OF RELATED CASES	1
JURISDICTIONAL STATEMENT	1
INTRODUCTION	2
STATEMENT OF THE ISSUES.....	4
STATEMENT OF THE CASE.....	5
A. The '452 Patent claims capture the novelty that dither signals and samples are processed by all the signal converters in the ADC pipeline.	5
B. Prior Art References.....	12
1. Cesura.....	12
2. Fu.....	15
3. Lewis	16
C. The <i>Inter Partes</i> Review Proceedings.....	17
1. The Board adopted a flawed claim construction that “said signal converters” can be less than all signal converters previously referenced in the same claim.....	17
2. The Board’s mistaken claim construction manifested in a flawed decision that prior art need only show samples being processed by <i>multiple</i> signal converters, but not <i>all</i> signal converters.	24
SUMMARY OF THE ARGUMENT	25
ARGUMENT	27
A. Standard of Review	27
B. The Board’s construction of “said signal converters” is erroneous because it departed from the ordinary meaning.	27
C. The intrinsic evidence supports the ordinary meaning of all “said signal converters”	33

D. The Board erroneously relied on the problem that the inventors encountered rather than the solution the inventors found as the basis for claim construction.....	35
E. None of the prior art references disclose processing the dither signals and samples by all the signal converters	39
CONCLUSION AND RELIEF SOUGHT	43

TABLE OF AUTHORITIES

	Page(s)
Cases	
<i>Baldwin Graphic Sys., Inc. v. Siebert, Inc.</i> , 512 F.3d 1338 (Fed. Cir. 2008)	27
<i>Harris Corp. v. Fed. Ex. Corp.</i> , 502 F. App'x 957 (Fed. Cir. 2013)	<i>passim</i>
<i>Homeland Housewares, LLC v. Whirlpool Corp.</i> , 865 F.3d 1372 (Fed. Cir. 2017)	27
<i>Leo Pharm. Prod., Ltd. v. Rea</i> , 726 F.3d 1346 (Fed. Cir. 2013)	38
<i>Process Control Corp. v. HydReclaim Corp.</i> , 190 F.3d 1350 (Fed. Cir. 1999)	<i>passim</i>
<i>Renishaw PLC v. Marposs Societa' per Azioni</i> , 158 F.3d 1243 (Fed. Cir. 1998)	27
<i>SciMed Life Sys., Inc. v. Advanced Cardiovascular Sys., Inc.</i> , 242 F.3d 1337 (Fed. Cir. 2001)	36
<i>United States v. CITGO Petroleum Corp.</i> , 801 F.3d 477 (5th Cir. 2015)	32
<i>United States v. Palmer</i> , 16 U.S. 610 (1818).....	32
Statutes	
28 U.S.C. § 1295(a)(4)(A)	1
35 U.S.C. § 6(b)(4).....	1
35 U.S.C. § 311	1

TABLE OF ABBREVIATIONS

Abbreviation(s)	Definition(s)
Analog	Appellant Analog Devices, Inc.
Xilinx	Appellees Xilinx, Inc. and Xilinx Asia Pacific Pte. Ltd.
'452 patent	U.S. Patent No. 7,719,452
Challenged Claims	Claims 1-4, 8, 9, 12-16, 19, and 20 of the '452 patent
Board or PTAB	United States Patent and Trademark Office Patent Trial and Appeal Board
ADC	Analog-to-Digital Converter
DAC	Digital-to-Analog Converter
Cesura	U.S. Patent No. 6,970,125
Fu	Daihong Fu et al., "A Digital Background Calibration Technique for Time-Interleaved Analog-to-Digital Converters," <i>IEEE Journal of Solid State Circuits</i> , Vol. 33, No. 12, Dec. 1998
Lewis	Stephen H. Lewis and Paul R. Gray, "A Pipelined 5-Msample/s 9-bit Analog-to-Digital Converter," <i>IEEE Journal of Solid State Circuits</i> , Vol. SC-22, No. 6, Dec. 1987

STATEMENT OF RELATED CASES

No appeal from the proceeding on U.S. Patent No. 7,719,452 (“’452 patent”) has been before this Court or any other court. Appellant Analog Devices, Inc. (“Analog”) has asserted claims of the ’452 patent against Xilinx, Inc. and Xilinx Asia Pacific Pte. Ltd. (“Xilinx”) in *Analog Devices, Inc. v. Xilinx, Inc. and Xilinx Asia Pacific Pte. Ltd.*, Case No. 1:19-cv-02225 in the United States District Court for the District of Delaware that may be affected by the Court’s decision.

JURISDICTIONAL STATEMENT

The U.S. Patent and Trademark Office had jurisdiction over the *inter partes* review (IPR) under 35 U.S.C. §§ 6(b)(4) and 311. The Board’s Final Written Decision was entered on March 11, 2022. Analog Devices (“Analog”) timely filed a notice of appeal on April 7, 2022. This Court has jurisdiction over this appeal under 28 U.S.C. § 1295(a)(4)(A).

INTRODUCTION

The Board’s decision turned on a flawed claim construction of the term “*said* signal converters.” The Board erred in its construction that “*said* signal converters” could be less than all of “signal converters” previously introduced in the same claim. The Board’s construction was not grounded in fact or law.

The ’452 patent relates to the field of circuits, and in particular a pipelined signal converter system for converting analog signals to corresponding digital codes. The ’452 patent utilizes a set of signal converters arranged in a sequence (or stages) to process the analog signals. And only after all of the signal converters process the input samples, an accurate output digital code that corresponds to the original sample is provided. The Board seemed to recognize the clarity of the ’452 patent. Appx16 (“we understand from a plain reading of the ’452 patent, that ‘using fewer than all the digital codes output by all the signal converters would result in digital output of the converter that does not correctly reflect the input analog signal.’”)

And the claims captured the novelty. The Challenged Claims introduce a set of “*signal converters* arranged and configured to successively process said samples.” And later in the same claim: “*said signal converters* which process said samples and said analog dither signals” and “said samples thus processed along different signal-processing paths of *said signal converters*.” The later-referenced

“said signal converters” are the *same set* of “signal converters” previously introduced in the same claim.

Yet the Board instituted the IPR petition on a misunderstanding that the claim “only requires that samples be processed along different signal-processing paths of *at least one* stage of the pipelined converter.” Appx10. In other words, the Board substituted “said signal converters” (plural) with “*at least one stage* of the pipelined converter.” Following institution, the Board clarified its construction, but again erred. The Board now concluded that “*said* signal converters” does not mean all of them, but could be a subset.

The Board thus reasoned that a prior art reference need only disclose signals processed through some signal converters—but not *all* those signal converters—to render the Challenged Claims invalid. But this Court has rejected the position that the Board adopted. This Court has emphasized that “*said*” encompasses the complete set of the original term and not just a subset. *See, e.g., Harris Corp. v. Fed. Ex. Corp.*, 502 F. App’x 957, 963-65 (Fed. Cir. 2013) (“*the . . . data*” means “*all* the aircraft data” and not just a “subset of the data”). The Board’s decision thus stands in contrast to this Court’s law.

Under proper construction, “*said* signal converters” means the same set of signal converters previously referenced in the same claim—not just some, a subset,

or a portion of the signal converters. Because the Board's mistaken claim construction manifested in a flawed decision, this Court should reverse.

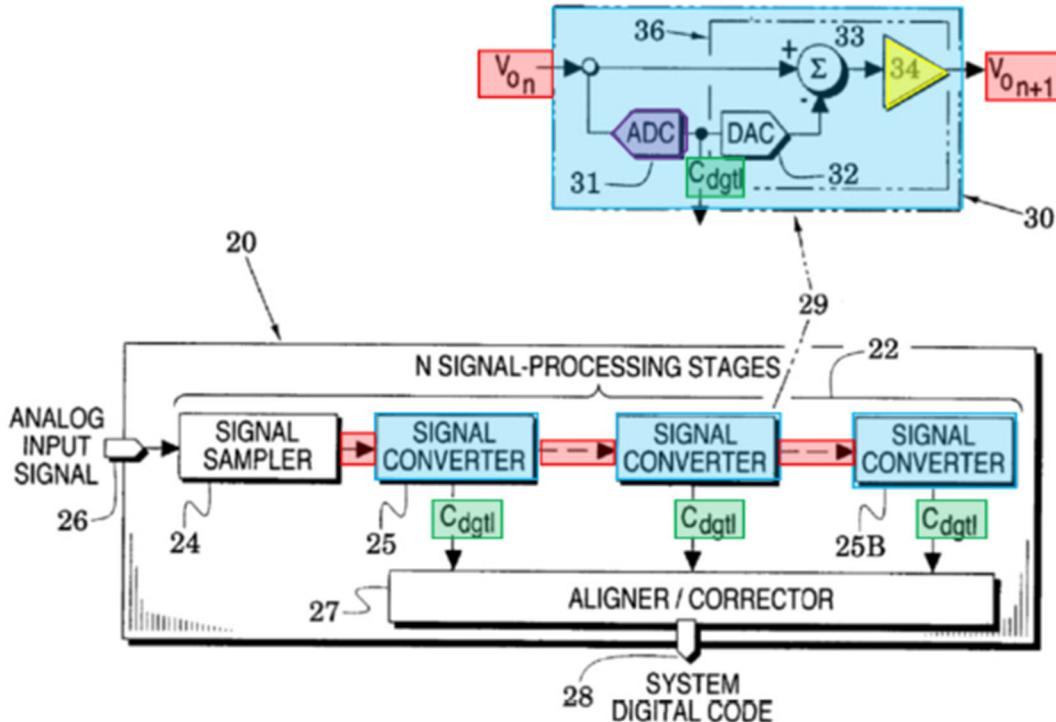
STATEMENT OF THE ISSUES

1. Did the Board err in its construction that "said signal converters" could be less than all of signal converters previously referenced in the same claim?
2. Whether, under proper construction of the term "said signal converters," the Board's unpatentability determinations are erroneous and unsupported by substantial evidence?

STATEMENT OF THE CASE

A. The '452 Patent claims capture the novelty that dither signals and samples are processed by all the signal converters in the ADC pipeline.

Analog-to-digital converters (“ADC”) convert analog signals into digital signals. Appx3. “Pipelined” or “multi-stage” ADC systems promote high-speed and high-resolution conversion. Appx76 at 1:10-14. Figure 1 of the '452 patent, reproduced below, shows an example of a pipelined ADC system consisting of a sampler and successive **signal converters 25** (also called “**stages**”). Appx1602 (Moon Decl.) at ¶14.



Id. (citing Appx65).

Each **signal converter** (or “**stage**”) of a pipelined system processes the **analog input signal** received from the immediately previous **stage** (or from the signal sampler, in the case of the first stage) and forms a **digitized version** (i.e., digital code C_{dgtl}) from that **analog input signal**. Appx1602 at ¶14. And “only after the aligner/corrector 27 has received the digital codes C_{dgtl} from *all of the signal converters* 25, does it provide a system digital code at an output port 28 that corresponds to the original sample.” Appx77 at 3:4-10 (emphasis added).

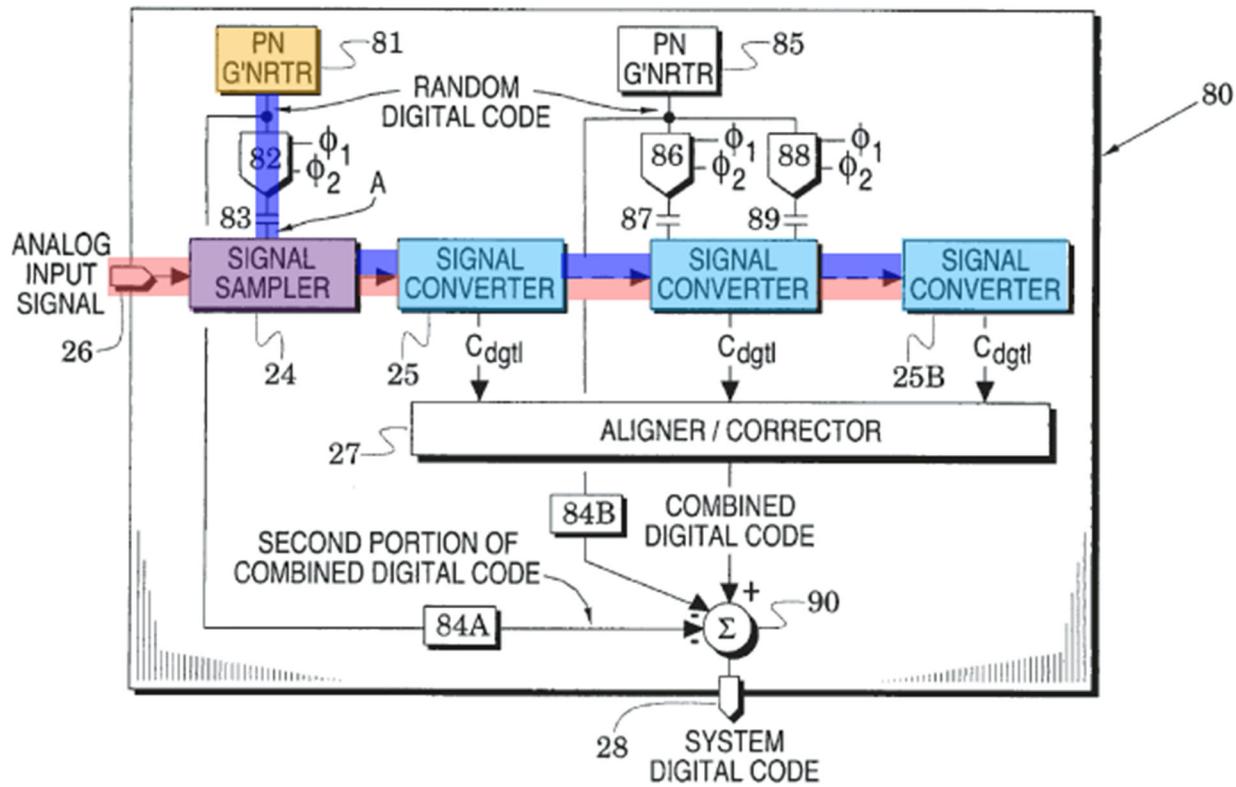
But ADC systems are also susceptible to errors that impact the accuracy of the signal conversion. Appx76 at 1:20-35. Each stage introduces some non-linearity errors that cause the output to deviate from a linear function corresponding to the input signal. Appx871-872 (Holberg Decl.) at ¶40. Introduction of non-linearities at each stage may be a function of fabrication errors that may impact the components of the digital-to-analog converter (“DAC”) portion of an ADC which leads to non-linear operation of the ADC. Appx5; Appx1610 at ¶24; Appx78 at 5:25-38. Other sources may also introduce various errors. Appx78 at 5:49-56. The goal of the '452 patent is to provide an ADC pipelined system with enhanced linearity that reduces the errors in the ADC conversion. Appx4; Appx76 at 1:51-52.

To account for these errors, the '452 patent injects an analog “dither” signal into the converter system, in a particular way. Appx64 at Abstract; Appx5-6. Dither signals are “noise” that, perhaps counterintuitively to a lay person, are intentionally added to the ADC system to improve the linearization effects. *See, e.g.*, Appx885-886 at ¶67; Appx1609 at ¶23. Dither addresses the non-linearity errors—not by correcting or accounting for root causes of a particular component’s error—but by randomizing the components that are used to process the input signals so that, on average, the errors in the different components of the ADC counteract each other, reducing the overall error in the conversion. Appx1610 at ¶24.

But the inventors of the '452 patent discovered that the linearization effect of the dither signal could be frustrated, or limited, in pipelined converters if the dither signal fails to reach all the signal converters. Appx1613 at ¶29. In such case, not all stages benefit from the randomizing and error-averaging effects of dithering. *Id.* And if the dither signal fails to reach the later signal converters, it would be as though dither was never injected from the perspective of the later stages. Appx1615 at ¶32.

Thus, the '452 patent modified the DAC components in a pipelined ADC to ensure that dither signal propagates through all the downstream signal converters

to improve linearity. Appx1613 at ¶30; Appx78 at 6:4-11. Figure 6 of the '452 patent, reproduced below, is one example of a pipelined ADC architecture that allows for injection of a dither signal that, along with samples of analog input signal, is processed by all the downstream signal converters. Appx6; Appx78 at 6:4-11.

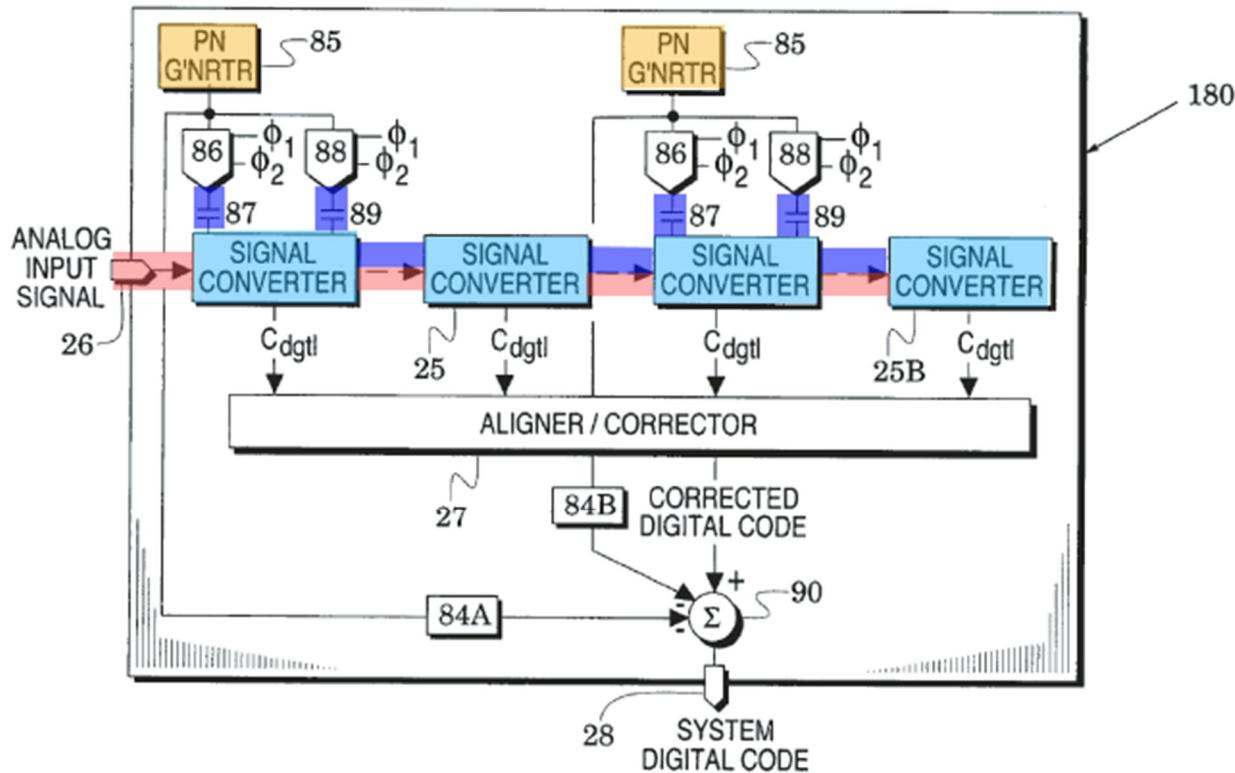


Appx68 (color added).

As shown above, the converter system 80 “couples a **pseudo-random (PN) generator** 81, a DAC 82 and at least one associated dither capacitor 83 to the **signal sampler** 24 for injection of **dither signals**” at entry point A of the **sampler**.

Appx78 at 6:7-16. The injected **dither signals** combine with the **analog input signal**, and the combined signal (i.e., both **analog input signal** and **dither signals**) is processed by each downstream **signal converter**. *Id.* at 6:16-22 (“the combined signal is processed down randomly-selected signal-processing paths of the converter system which induce different magnitudes and signs of INL [integral nonlinearity] errors.”). The specification emphasizes that “[i]t is important to note . . . that these linearity improvements are realized by simultaneous processing of two combined analog signals—the input signal at the input port 26 and the injected dither signal.” *Id.* at 6:23-26. The processing of the signals by each signal converter “provides a combined digital code at the output of the aligner/corrector 27.” *Id.* at 6:26-28. And in “a different system embodiment, similar linearity improvements are realized with dither signals that are injected in a selected downstream signal converter.” *Id.* at 6:44-46.

In other configurations of pipelined ADC system, a sampler can be removed. Appx82 at 14:52-54 (“without a signal sampler . . . it reduces power demand and reduces the output distortion and noise of the system 80.”). Figure 10, reproduced below, discloses multiple insertions points of **dither signals** directly into the **signal converters** (at the first stage and a successive stage) in a system that are then processed by each signal converter in the system:



Appx74 (color added).

Independent claims 1 and 13, reproduced below with relevant emphasis for key limitations, capture the invention discussed above. The dispute in this appeal focuses on “said signal converters” in each independent claim:

Claim 1: [1A] An analog-to-digital converter system to convert an analog input signal to a system digital code, comprising:

[1B] a sampler to provide samples of said analog input signal;

[1C] ***signal converters*** arranged and configured to successively process said samples;

[1D] at least one digital-to-analog converter configured

to respond to a random digital code and *inject analog dither signals into at least a selected one of said sampler and said signal converters which process said samples and said analog dither signals* into a plurality of digital codes;

[1E] an aligner/corrector coupled to said signal converters to process said plurality of digital codes into a combined digital code that includes a first portion that corresponds to said samples and a second portion that corresponds to said analog dither signals; and

[1F] a decoder having a transfer function configured to convert said random digital code to said second portion for differencing with said combined digital code to thereby provide said system digital code;

[1G] *said samples thus processed along different signal-processing paths of said signal converters* to thereby enhance linearity of said system.

Appx83 at 15:63-16:18 (emphasis added).

Claim 13: [13A] An analog-to-digital converter system to convert an analog input signal to a system digital code, comprising:

[13B] **signal converters** arranged and configured to provide and successively process samples of said analog input signal;

[13C] at least one digital-to-analog converter configured to respond to a random digital code and *inject corresponding analog dither signals into at least a selected one of said signal converters to enable said selected signal converter and succeeding signal converters to successively process said analog dither*

signals, processing of said samples and said analog dither signals thereby generating a plurality of digital codes;

[13D] an aligner/corrector coupled to said signal converters to process said plurality of digital codes into a combined digital code that includes a first portion that corresponds to said samples and a second portion that corresponds to said analog dither signals; and

[13E] a decoder having a transfer function configured to convert said random digital code to said second portion for differencing with said combined digital code to thereby provide said system digital code;

[13F] *said samples thus processed along different signal-processing paths of said signal converters* to thereby enhance conversion linearity of said system.

Appx84 at 17:4-28 (emphasis added).

B. Prior Art References.

The three references that Xilinx and the Board relied upon for independent claims 1 and 13 are U.S. Patent No. 6,970,125 to Cesura *et al.* (“Cesura”) (Appx1218-1227) for “Ground A” challenge, and non-patent literatures to Fu (Appx1228-1235) and Lewis (Appx1236-1243) for “Ground C” challenge. Appx17; Appx19; Appx48.

1. Cesura

Cesura is titled “Multistage Analog-to-Digital Converter” and relates to an ADC converter having a pipeline architecture. Appx1218; Appx1222 at 1:7-8. Cesura noted that in pipeline architecture, each stage performs a successive

approximation of the digital signal and generates residue that is then passed to the next stage in the pipeline. Appx1222 at 1:19-25. And “the residues are amplified by a pre-set analog gain before being passed to the next stages; in this way, each stage operates with a similar input signal range.” *Id.* at 1:28-30.

The problem that Cesura identified with the residues was that “any error in the (inter-stage) gain causes a harmonic distortion in the digital signal generated by the converter.” *Id.* at 1:31-32. “This problem is particular acute in the first stages of the pipeline” and imprecision of the inter-stage gain reduces the actual resolution that can be achieved. *Id.* at 1:33-39.

To address this gain error problem, Cesura discloses supplementing the first converter stage of the ADC with a “combining circuit” that includes “a circuit for dynamically estimating a digital correction signal indicative of an analog error of the corresponding inter-stage gain.” Appx1218 at Abstract; Appx1224 at 6:24-29 (“In the converter of the invention the means for combining includes, for one or more of the stages, means for dynamically estimating a digital error indicative of an analog error of the corresponding analog gain”).

Figure 2, reproduced below, shows a system that implements Cesura’s error estimation technique by supplementing the first converter stage of the ADC pipeline with a “**combining circuit**” (Appx1633):

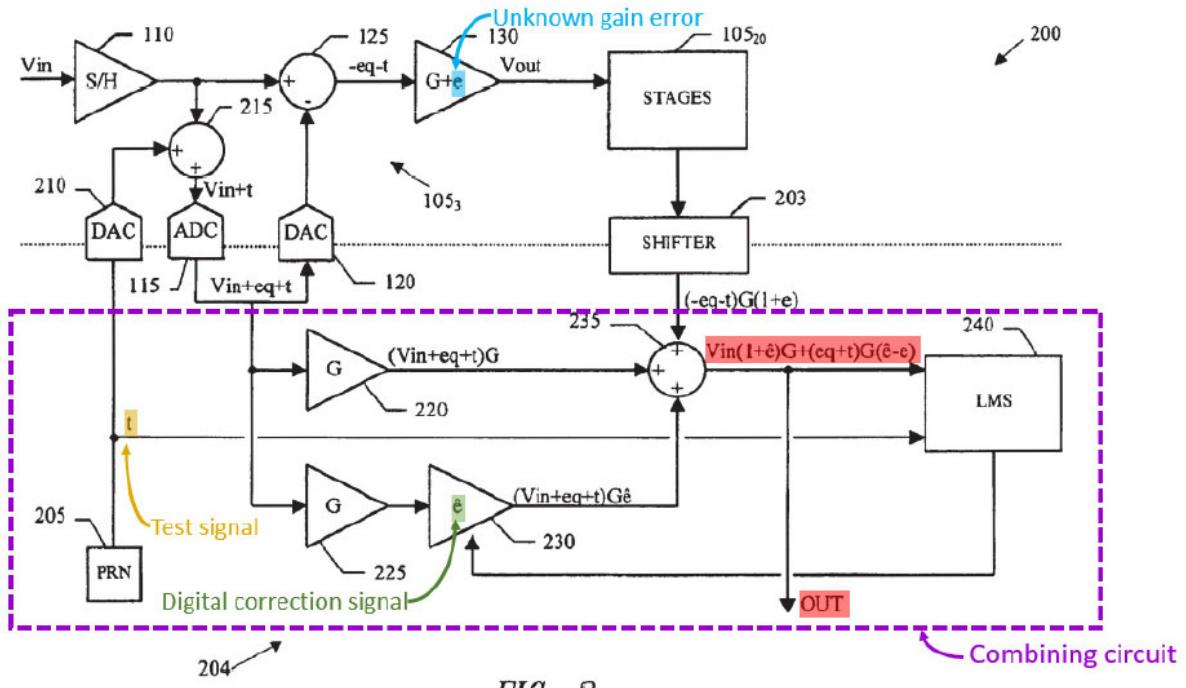


FIG. 2

Appx1633; *see also* Appx1220.

In the figure above, the actual gain error in the first stage amplifier 130 is shown as “e” and is unknown. Appx1633-1634 at ¶61. Cesura attempts to estimate and correct that error by generating a digital correction signal, shown as “ \hat{e} ” in the figure, by correlating a random **test signal** “ t ” with the output (“**OUT**”) of the ADC. *Id.* Thus, what Cesura invented was using a test signal “ t ” to estimate and compensate for the gain error at the first stage.

Although nowhere in the references does Cesura state or equate “t” with a dither signal, Xilinx argued that the test signal “t” is equivalent to the dither signal of the ’452 patent. Appx181; Appx920 at ¶106. And Xilinx, along with its expert,

stated “that Cesura’s analog dither signals [t] will cause *at least one stage* of its pipelined ADC to operate at different operating points, depending on the value of the dither signal at any given moment.” Appx181; Appx920 at ¶106 (emphasis added).

2. Fu

Fu is non-patent literature that discloses a method of calibrating mismatched gain errors in ADCs. Appx1228 at Introduction; Appx49-50. Like Cesura, Fu’s calibration method requires injecting a random analog value into an ADC and then monitoring and correlating its output to the test signal to estimate the gain. Appx1650.

Fu’s system describes time interleaving multiple ADCs to achieve a faster sampling rate than provided by a single ADC. *Id.* Fu’s gain calibration system discloses inserting a random analog value using a **summing nodes** located before the pipelined ADC stages:

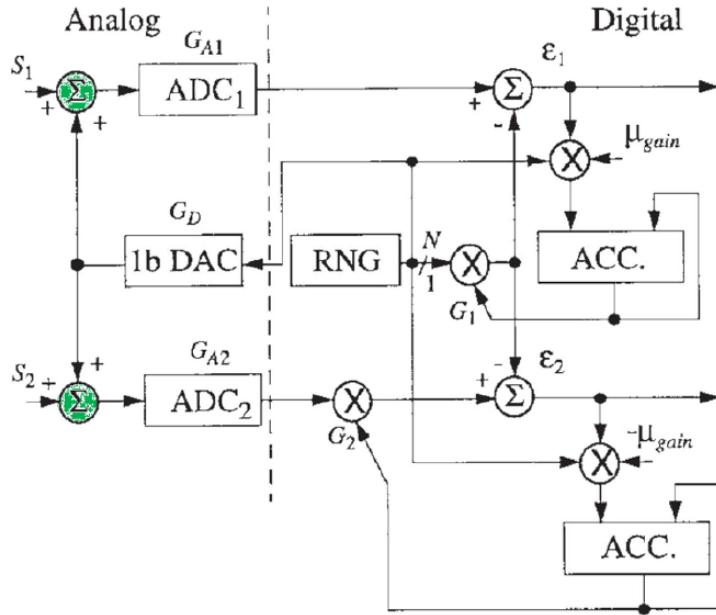


Fig. 4. Modified gain calibration system for two time-interleaved ADC's.

Appx1651-1652 at ¶87.

And similar to Cesura, Xilinx and its expert argued that “Fu’s analog dither signals will cause *at least one stage* of its pipelined ADC to operate at different operating points, depending on the value of the dither signal at any given moment.”

Appx226-227 (emphases added); Appx984-985 at ¶200.

3. Lewis

Lewis is non-patent literature titled “A Pipelined 5-Msample/s 9-bit Analog-to-Digital Converter.” Appx1236. According to Xilinx, Lewis provides circuit details that Fu omits. Appx206 (“The combination of Fu with Lewis . . . is really nothing more than using Lewis’ . . . detailed disclosure to fill in details that Fu presumably considered too well-known and/or too trivial to provide Hence,

Lewis is simply an explanation of what a POSITA would have understood the disclosure of Fu to include.”); Appx954 at ¶159; Appx1653 at ¶90.

Xilinx did not rely upon Lewis for the disclosure of dither signal insertion or processing signals “along different signal-processing paths of said signal converters.” Thus, Lewis is not the basis of any limitations subject to this appeal.

C. The *Inter Partes* Review Proceedings

Xilinx petitioned for *inter partes* review (IPR) to challenge certain claims of the '452 patent on multiple grounds. Appx17. For independent claims 1 and 13, Xilinx relied on two grounds: (1) single reference obviousness based on Cesura, and (2) a combination of Fu and Lewis. *Id.*

- 1. The Board adopted a flawed claim construction that “said signal converters” can be less than all signal converters previously referenced in the same claim.**

Neither party had sought any claim construction for any term. Appx329. Petitioner Xilinx had indicated that all terms should be given their plain and ordinary meaning. Appx169. And Patent Owner Analog, in its preliminary response, similarly never raised any claim construction for any term. Appx329. But when presented evidence that the prior art references failed to disclose all the key limitations, the Board impermissibly broadened the claim scope of the '452 patent using its flawed claim construction.

During the IPR proceeding, Analog highlighted that the prior art references provided no insight regarding the problem that the '452 patent was addressing in conventional systems (i.e., the dither signal failed to reach all the signal converters in the pipeline). *See, e.g.*, Appx292-296; Appx308-311. And the prior art had failed to disclose the “said signal converters which process said samples and said analog dither signals into a plurality of digital codes” and processing samples “along different signal processing paths of said signal converters.” Appx283-284. In each instance, the “said signal converters” refers to the same set of “signal converters arranged and configured to successively process [said] samples” in earlier limitation [1C]. *Id.*

The term “signal converters” appears three times in independent claim 1:

[1C] **signal converters** arranged and configured to successively process said samples;

[1D] at least one digital-to-analog converter configured to respond to a random digital code and *inject analog dither signals into* at least a selected one of said sampler and **said signal converters which process said samples and said analog dither signals** into a plurality of digital codes;

...

[1G] **said samples thus processed along different signal-processing paths of said signal converters** to thereby enhance linearity of said system.

Appx83 at 15:63-16:18 (emphasis added).¹

Claim 1 captured the novelty disclosed in both Figures 6 and 10 (reproduced below), where a **dither signals** can be introduced into the ADC pipeline either via **sampler** (Fig. 6) or directly into **a signal converter** (Fig. 10), when sampler is not present. Appx25 (“The parties acknowledge . . . that in claim [1D] dither can be injected into either the sampler or one of the signal converters.”); Appx189 (Petition) (“in [1D] dither can be injected into either the sampler or one of the signal converters, whereas in [13C] dither must be injected into one of the signal converters.”); Appx412.

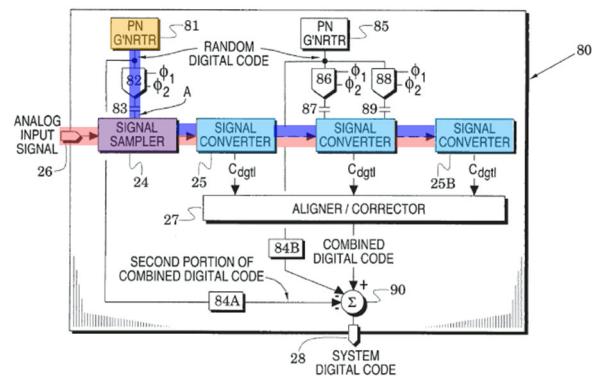


Fig. 6; Appx68 (color added).

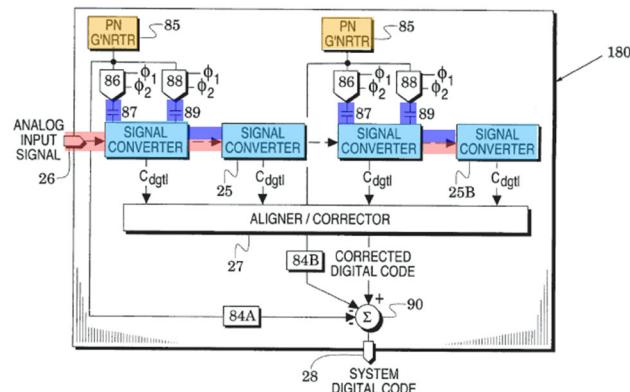


Fig. 10; Appx74 (color added).

¹ Similar limitations are recited in independent claim 13 with minor variation as to the insertion point for the dither signal. Appx84 at 17:4-28; Appx25.

But the Board, as part of its Institution Decision, suggested “that claim 1 ‘only requires that samples be processed along different signal-processing paths of **at least one stage** of the pipelined converter.’” Appx10 (emphasis added); Appx342-343. The Board justified its decision by parsing limitation 1[D] that discusses the insertion point of the dither signal into the converter system. Appx342. The Board suggested that 1[D] limitation “can be reasonably understood to mean that dither signals are injected into ‘a selected one of . . . said signal converters which process said samples’ and not necessarily into ‘each’ of the pipelined signal converters.” *Id.* But 1[D] is the point of insertion for the dither signal into the system (either the sampler or a signal converter). Once the dither signal is inserted into the ADC system, the claims specify that “said signal converters which process said samples and analog dither signals” and later note “said samples thus processed along different signal-processing paths of said signal converters.”

By importing the limitation of “at least one” from 1[D] related to the injection point of the dither signal into either a sampler or signal converter, the Board reasoned that the challenged claim require processing the samples along only “**at least one** stage of the pipelined converter.” *Id.* (emphasis added). And as such, the Board went down the wrong path. The parties addressed the Board’s

construction following institution. Appx395-406 (Patent Owner's Response); Appx455-459 (Petitioner's Reply); Appx482-486 (Patent Owner's Sur-Reply).

In the final written decision, the Board “clarified” its construction. Appx10; Appx17. The Board acknowledged that “said signal converters” in 1[G] is plural and the antecedent basis for that term is found in limitation 1[C] that recites “*signal converters* arranged and configured to successively process [said] samples.” Appx11. However, the Board maintained that limitations 1[G] and 13[F] are “not limited to, or properly interpreted as, processing samples along ‘*all* said signal converters’ in the claimed analog-to-digital converter systems.” Appx17. The Board’s rationale for its construction hinged on two premises.

First, the Board faulted Analog for allegedly not having written the claim more clearly despite no party having raised its ambiguity before institution and despite the support in the specification. The Board suggested that while “the invention was *clearly discussed* in the Specification of the ’452 patent, it would have been an elementary matter for the claim to have been similarly drafted to specify this limitation, e.g., by writing the limitation as ‘*all* said signal converters,’ or alternatively ‘*each of* said signal converters.’” Appx12 (emphasis added). But as elaborated below, Analog also did not write the claim to state that “said signal

converters” was “*a subset of* said signal converters.” Yet the Board construed limitations 1[G] and 13[F] as such.

Second, the Board rationalized its claim construction based on the erroneous conclusion that “both Figures 7A and 7B are embodiments of the signal converting structure shown in Figure 6.” Appx14. But Figure 7A showed the *problem* that the inventors of the ’452 patent encountered with dither signals failing to reach all signal converters. Appx79 at 7:52-57 (“It is apparent from FIG. 7A, however, that the operating point in subsequent stages 3-5 remains at the operating point prior to application of dither. . . . Thus, the dither fails to alter the signal processing path through these latter stages.”). Figure 7A, reproduced below, shows that the dither signal failed to reach the later signal converter stages 3-5 (in red):

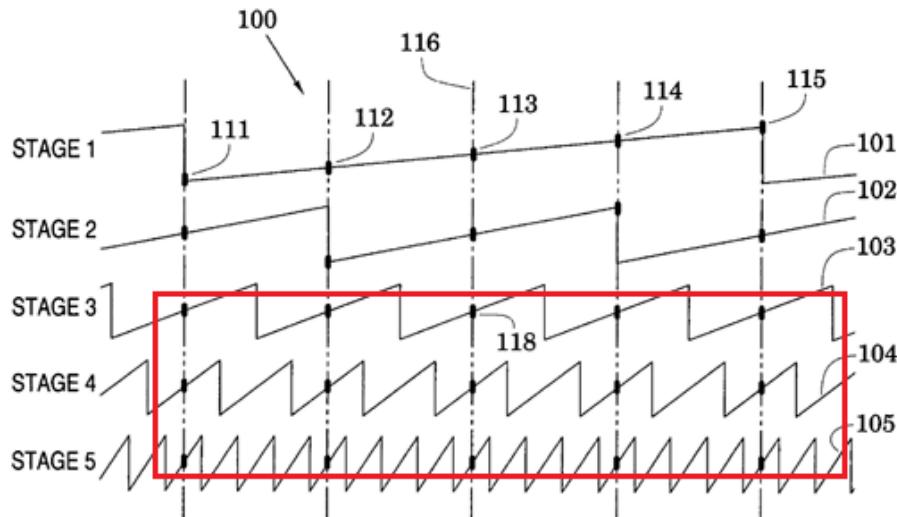


FIG. 7A

Appx69 (annotated); Appx79 at 7:54-57 (“In the third stage, for example, operating points such as the point 118 remain at the center of the converter subrange” and therefore “the dither fails to alter the signal processing path through these latter stages.”). But “[t]his failure is removed in the dither arrangements exemplified in FIGS. 7B and 7C” (*Id.* at 7:57-59) as shown below:

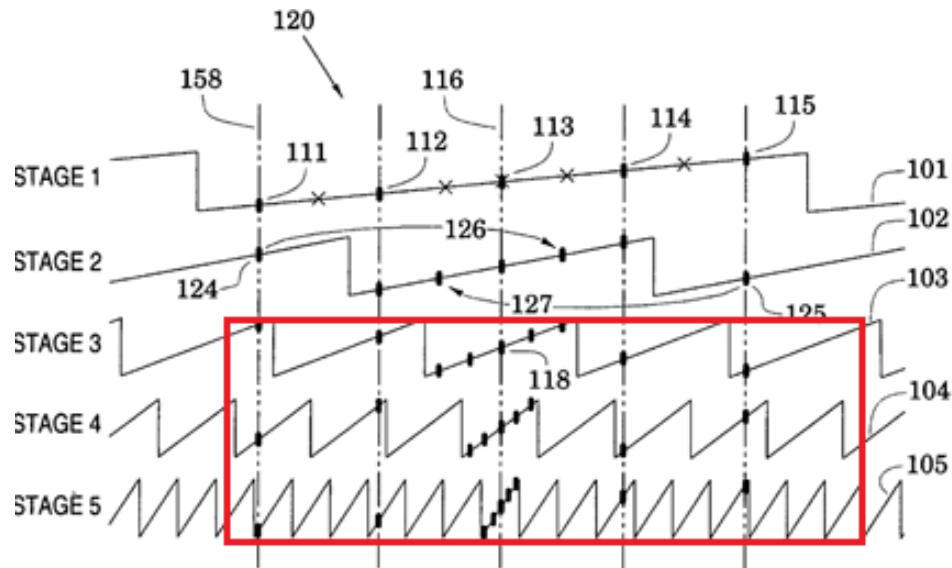


FIG. 7B

Appx70 (annotated).

“This is *an important contrast* to the situation in FIG. 7A in which there was an absence of dither range in the third, fourth and fifth stages. The applied dither now establishes different signal processing paths *throughout all* stages of FIG. 7B.” Appx79 at 8:35-39 (emphasis added).

Because Figure 7A was not explicitly marked as prior art—even though it explained the problems that inventors of the '452 patent discovered—the Board

suggested that “Figure 7A is mainly described as a less preferred embodiment of the converter system shown in Figure 6 where ‘dither exhaustion’ may occur.” Appx15. Thus, the Board construed “said signal converters” in 1[G] to be less than all of “signal converters” referenced in the same claim in limitations 1[C].

In sum, the result of the Board’s clarification from institution stage to the final decision was the same: the claim scope of “said signal converters” had been improperly modified from its full scope to less than all converters to accommodate the prior art references.

2. The Board’s mistaken claim construction manifested in a flawed decision that prior art need only show samples being processed by *multiple* signal converters, but not *all* signal converters.

The Board’s erroneous construction caused it to invalidate the Challenged Claims. Analog had argued that neither Cesura (Ground A) nor the Fu and Lewis combination (Ground C) discloses the limitation of “said samples thus processed along different signal-processing paths of *said signal converters*.” Appx25-28; Appx52-53.

While acknowledging that the specification of the ’452 patent was directed to ensuring that an injected dither signal would propagate to each converter stage in the pipeline, the Board still dismissed Analog’s validity objections on the basis of claim construction. Appx30 (“we agree with Patent Owner’s statement that ‘as

the inventors observed, the use of such specific configurations of dither signals could ensure that an injected dither signal would propagate to *each* converter stage in the pipeline.’ In any event, as discussed above, the proper claim construction for limitation 1[G] is not limited to processing samples along ‘*all* said signal converters’ in the claimed analog-to-digital converter system.”) (emphasis added).

Thus, for Ground A, the Board was satisfied “that Cesura’s test signal *t* is applied to *multiple stages* of the signal converter system,” even if not *all* of the signal converters. Appx34 (emphasis added); Appx35. The Board similarly rejected Analog’s objections on Fu and Lewis combination (Ground C) because the Board erroneously concluded that the claims do not require the analog signal to be processed along different signal-processing paths “of *each* of the *multiple* signal converters in the analog-to-digital converter.” Appx53 (emphasis in original).

The Board’s ultimate validity conclusions were wrong because they stemmed from an improper claim construction.

SUMMARY OF THE ARGUMENT

The Board’s construction of “said signal converters” for claims 1 and 13 of the ’452 patent wrongly departed from the ordinary meaning of the phrase. This Court has emphasized that even without “all” in the claim, the use of “the” and “said” means that the later phrase encompasses *all* of the original set. *Harris*, 502

F. App'x at 963-65. Here, the introduction of “*signal converters* arranged and configured to successively process said samples” defined a set of signal converters. All later references to “said signal converters” mean the *same* set of signal converters originally defined.

The Board, however, turned what was an uncontested and ordinary phrase upside down. The Board conceded that “said signal converters” refers to a plurality of signal converters (i.e., a set of signal converters) and finds its antecedent basis in the preceding limitation. Appx11. The Board also appreciated the clarity of the specification. Appx12 (“this feature, or embodiment, of the invention was *clearly discussed* in the Specification of the ’452 patent”); Appx16 (“we understand from *a plain reading of the ’452 patent*, that ‘using fewer than all the digital codes output by all the signal converters would result in digital output of the converter that does not correctly reflect the input analog signal.’”) (emphasis added). Yet the Board remained unpersuaded that the “said signal converters” was the same set of signal converters introduced earlier. Appx11.

The Board’s misguided distraction was Figure 7A, which instead of an embodiment, illustrates the *problem* that the inventors encountered and solved. Appx10-11; Appx15; Appx79 at 7:52-57. The solution to the problem was shown in Figures 7B and 7C. Appx79 at 7:57-59. But the Board’s “attempt to use the

written description to circumvent the plain language of the claim and the clear definition of the disputed claim language found therein was inappropriate.” *Process Control Corp. v. HydReclaim Corp.*, 190 F.3d 1350, 1357 (Fed. Cir. 1999). Thus, the Board ignored the plain meaning and construed “said signal converters” to encompass the very problem that the inventors discovered and were addressing. Appx14-15. And based on the flawed construction, the Board held that the prior art need only disclose samples being processed by multiple signal converters, but not all signal converters, finding that Cesura and Fu satisfied that requirement. The Board thus erred.

ARGUMENT

A. Standard of Review.

This Court reviews the Board’s conclusions of law *de novo* and its findings of fact for substantial evidence. *Homeland Housewares, LLC v. Whirlpool Corp.*, 865 F.3d 1372, 1374 (Fed. Cir. 2017). Claim construction is a question of law that this Court reviews *de novo* when, as here, the Board’s construction did not rely on any extrinsic evidence. *Id.*

B. The Board’s construction of “said signal converters” is erroneous because it departed from the ordinary meaning.

“The claim construction inquiry . . . begins and ends in all cases with the actual words of the claim.” *Renishaw PLC v. Marposs Societa’ per Azioni*, 158

F.3d 1243, 1248 (Fed. Cir. 1998). This should have been the case with “said signal converters.”

This Court has repeatedly held that later uses of definite articles “the” or “said” in a claim refer to the same claim term introduced earlier. *Baldwin Graphic Sys., Inc. v. Siebert, Inc.*, 512 F.3d 1338, 1342 (Fed. Cir. 2008). Their use does not alter the claim scope of the term. *Process*, 190 F.3d at 1356 (“the term ‘a discharge rate’ in [earlier] clause . . . is referring to the same rate as the term ‘the discharge rate’”). Indeed, when identical terms are used along with “the” or “said,” it “is not a case where the claim language is reasonably susceptible to two constructions. Rather, the claim as written by the patentee is susceptible to only one meaning.” *Id.* Maintaining a consistent claim scope “avoids any lack of antecedent basis problem for the occurrence of” the later use of the same term. *Id.* at 1356-57. The Board acknowledged that the antecedent basis for “said signal converters” is found in the earlier clause (Appx11), but still construed the later term as not requiring all of the same signal converters. This construction was erroneous. Appx17.

The express words of the ’452 patent claims chosen by the patentee are specific and unambiguous. Neither Xilinx nor Analog had requested any construction or clarification of its meaning. Appx169; Appx329. The initial introduction of “signal converters” in limitations [1C] and [13B] of claims 1 and

13 respectively defined the scope: “signal converters arranged and configured to successively process said samples.” Appx83 at 15:63-16:18; Appx84 at 17:4-28. Each of the later “said signal converters” refers to the *same set* of signal converters. The Board erred because it saw ambiguity where there was none. *Process*, 190 F.3d at 1357 (“Where, as here, the claim is susceptible to only one reasonable construction . . . we must construe the claims based on the patentee’s version of the claim as he himself drafted it.”).

But even if the term “said signal converters” could be amenable to multiple constructions—it is not—the only construction that stays true to the ordinary meaning and intrinsic evidence is Analog’s. This Court’s decision in *Harris* is instructive. *Harris*, 502 F. App’x at 957. In *Harris*, the Court reversed the district court’s construction because this Court held that the disputed term “*the* accumulated, stored generated aircraft data” should have been construed as “***all*** the aircraft data” based on the natural reading of the claim. *Id.* at 965 (emphasis in original). “This is especially true where, as here, the later instance refers to ‘the’ data and therefore begs for some antecedent basis.” *Id.* at 963.

In *Harris*, the accused infringer argued “that nothing in this language requires that ‘all’ of the data . . . must be transmitted . . . and accuses [patentee] of importing the word ‘all’ into the claim in the absence of support for such an

inclusion.” *Id.* The accused infringer sought its construction of “the . . . data” because its design-around system transmitted less than “all” of the accumulated data. *Id.* at 962. Here, too, the prior art references that Xilinx relied on signal processing using less than “all” of the signal converters. But this Court rejected this argument for two reasons. *Id.* at 963.

“First, although the claim does not expressly require that ‘all’ of the accumulated data must be transmitted, it similarly lacks any indication that some subset of the accumulated data should be transmitted, and if so what that subset should be. In the absence of such guidance, [patentee’s] interpretation seems entirely reasonable.” *Id.* And second, the accused infringer’s construction would have required “the . . . data” to mean “a subset of the data” as the alternative construction. *Id.* Thus, with “competing constructions that each import additional language into the claim,” this Court concluded that it was the patentee’s “all” construction that “most naturally aligns with the claim language.” *Id.* at 963-64.

The *Harris* principles also apply here with “said signal converters” for two reasons. First, the claims never suggest that “*a subset of* said signal converters” can process the samples, and if so what that subset would be. The lack of guidance in the claim for which “*subset of* said signal converters” could process the samples is magnified by the Board’s equivocation. In the institution decision, the Board

concluded that the disputed limitation “only requires that samples be processed along different signal-processing paths of *at least one* stage of the pipelined converter.” Appx10 (emphasis in original). And in the final decision, the Board held that the limitation “is not limited to, or properly interpreted as, processing samples along ‘*all* said signal converters’ in the claimed analog-to-digital converter systems.” Appx17 (emphasis in original). Thus, the “subset” could be anything between “*at least one*” and less than “*all*” signal converters. The inability of the Board to identify which subset of signal converters could process the samples highlights the Board’s erroneous construction.

Second, the natural reading of claim language reciting “*said signal converters*” confirms that the samples and analog dither signals are processed by the same set of signal converters introduced earlier (“*signal converters arranged and configured to*”). For example, limitation [1D] requires injecting the analog dither signals “*into at least a selected one of said sampler and said signal converters which process said samples and said analog dither signals into a plurality of digital codes.*” Appx83 at 15:63-16:18. And limitation [1G] requires that “*said samples thus processed along different signal-processing paths of *said signal converters* to thereby enhance linearity of said system.*” *Id.* at 16:16-18 (emphasis added).

The Board suggested that limitation [1D] “can be reasonably understood to mean that dither signals are injected into ‘a selected one of . . . said signal converters which process said samples’ and not necessarily into ‘each’ of the pipelined signal converters.” Appx342. Although the dither signal can be introduced from the ADC pipeline directly into one of said signal converters, as shown in Figure 10 of ’452 patent, the Board erred by then taking that introduction of the dither signal into the system and suggesting that only one (or less than all) said signal converters *process* the dither signal.

Limitation [1D] does not stop at the injection of the dither signal. Claim 1 recites: “said signal converters *which* process said samples and said analog dither signals into a plurality of digital codes.” The word “which” is a relative pronoun that refers to the nearest antecedent noun (i.e., said signal converters). *See, e.g., United States v. Palmer*, 16 U.S. 610, 618 (1818) (In interpreting a statue, finding that the use of the “relative pronoun which” refers to the immediate antecedent); *United States v. CITGO Petroleum Corp.*, 801 F.3d 477, 484 (5th Cir. 2015) (“The relative pronoun ‘which’ refers to the noun immediately preceding it”). Thus, the natural reading of the limitation is: “all of said signal converters which process said samples and said dither signals,” and *not* how the Board construed it: “one of . . . said signal converters process said samples and said dither signals.”

The Board appeared to understand the inventive concept of the '452 patent, but construed the claims contrary to their ordinary meaning. *See Appx12* (“[T]he invention was *clearly discussed* in the Specification of the '452 patent, it would have been an elementary matter for the claim to have been similarly drafted to specify this limitation, e.g., by writing the limitation as ‘*all* said signal converters,’ or alternatively ‘*each of* said signal converters.’”) (emphasis added). The Board cannot alter the claim scope because a term was not written to the Board’s stylistic preference. The presence of the identical language in limitations [1C], [1D], and [1G] *and* [13B], [13C], and 13[F] shows that the patentee referred to the *same set of* signal converters. *See Process*, 190 F.3d at 1356; *Harris*, 502 F. App’x at 963 (“When identical language is found in multiple steps within the same claim, it is reasonable to assume that all references relate to the same subject matter.”).

For these reasons, the Board erred in its construction of “said signal converters” when it deviated from the ordinary meaning of the phrase.

C. The intrinsic evidence supports the ordinary meaning of all “said signal converters.”

The intrinsic evidence supports the construction that “said signal converters” means *all* signal converters, even if the Board’s “attempt to use the written description to circumvent the plain language of the claim and the clear definition of

the disputed claim language found therein was inappropriate.” *Process*, 190 F.3d at 1357.

Here, the specification confirms that the signal is processed through *all* the signal converters (i.e., “stages”). *See, e.g.*, Appx79 at 8:37-39 (“The applied dither now establishes different signal processing paths *throughout all stages*”); Appx82 at 14:39-42 (“In a feature of the present disclosure, however, dither points *propagate through the converter stages*”) (emphasis added). And the “combined signal” that includes both the injected dither signal and the analog signal is “processed down randomly-selected signal-processing paths of *the remaining converter stages*,” referencing each converter stage in the converter system. Appx82 at 14:5-9 (emphasis added). The “dither capacitors are [also] preferably sized to adjust the predetermined dither range to enhance this portion in the selected stage *and in each of succeeding signal converters*.” Appx81 at 12:21-23 (emphasis added).

Even the Board acknowledge that “we understand from *a plain reading of the '452 patent*, that ‘using fewer than *all* the digital codes output by *all the signal converters* would result in digital output of the converter that does not correctly reflect the input analog signal.’” Appx16 (emphasis added); *see also* Appx12.

Thus, the specification supports the construction that “said signal converters” referred to all of the same signal converters.

In *Harris*, “nothing in the specification indicate[d] that ‘all’ data accumulated during the flight must be transmitted,” but this Court still held that “the . . . data” meant “*all* the aircraft data.” *Harris*, 502 F. App’x at 964. The intrinsic support in the ’452 patent, however, does show the use of all converters in order to solve the problem faced by the inventors. And the specification does not support any alternative construction where “said signal converters” means anything less than all signal converters. Thus the Board erred.

D. The Board erroneously relied on the problem that the inventors encountered rather than the solution the inventors found as the basis for claim construction.

The Board’s only rationale for its construction was the very problem that the inventors discovered and ultimately solved. Appx12-16. The Board, however, used the disclosure of the problem as the basis to expand the claim scope of the solution, by labeling the problem a “less preferred embodiment.” Appx14-15.

Here, the Board turned a situation that the inventors found as undesirable (where there is no dither in later stages) into another embodiment captured by the claims. But this is not proper. “Where the specification makes clear that the invention does not include a particular feature, that feature is deemed to be outside the reach of the claims of the patent, even though the language of the claims, read

without reference to the specification, might be considered broad enough to encompass the feature in question.” *SciMed Life Sys., Inc. v. Advanced Cardiovascular Sys., Inc.*, 242 F.3d 1337, 1341 (Fed. Cir. 2001).

The specification of the '452 patent noted that “[i]t is apparent from FIG. 7A, however, that the operating point in subsequent stages 3-5 remains at the operating point prior to application of dither.” Appx79 at 7:52-54; Appx27. Figure 7A, reproduced below, shows that the dither signal failed to reach the later signal converter stages 3-5 (in red):

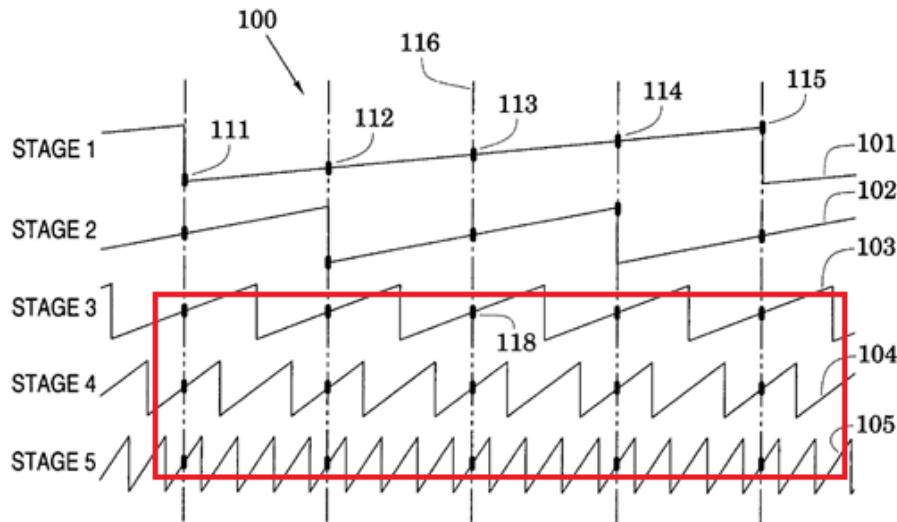


FIG. 7A

Appx69 (annotated).

“In the third stage, for example, operating points such as the point 118 remain at the center of the converter subrange” and therefore “the dither fails to alter the signal processing path through these latter stages.” Appx79 at 7:54-57. In

other words, a dither value that was not sufficiently high would fail to reach each signal converter through the ADC pipeline structure. But “[t]his failure is removed in the dither arrangements exemplified in FIGS. 7B and 7C” (*id.* at 7:57-59) as shown below:

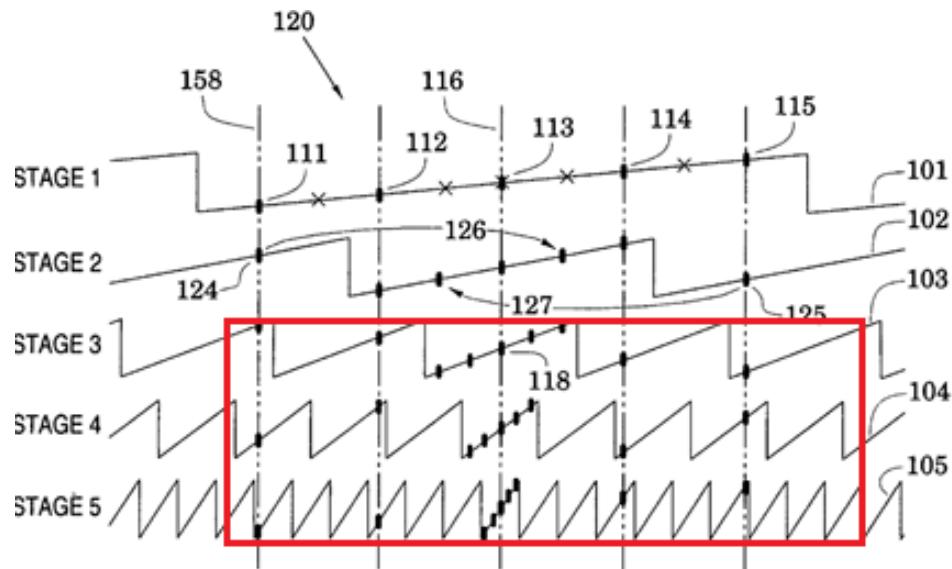


FIG. 7B

Appx70 (annotated).

“This is *an important contrast* to the situation in FIG. 7A in which there was an absence of dither range in the third, fourth and fifth stages. The applied dither now establishes different signal processing paths *throughout all* stages of FIG. 7B.” Appx79 at 8:35-39 (emphasis added).

The Board, however, used the problem that was identified by the inventors to suggest that Figure 7A was simply “a less preferred embodiment” to Figure 7B. Appx14-15. And because “the ’452 patent does not describe Figure 7A as

representative of the prior art,” the Board construed “said signal converter” to be less than all signal converters. Appx15. In effect, the Board’s construction captured the problem discussed in the ’452 patent so that the prior art references did not need to disclose the claimed solution in order to invalidate the claims. But a problem that the inventors uncover is not necessarily “prior art.” *Leo Pharm. Prod., Ltd. v. Rea*, 726 F.3d 1346, 1353 (Fed. Cir. 2013) (“an invention can often be the recognition of a problem itself.”) (internal citation omitted).

Here, until the problem with a dither signal failing to reach all signal converters was identified by the inventors of the ’452 patent, the possible approaches to solving the problem were not known, and the solution was not predictable. The Board, however, labeled the problem that the inventors identified as a “less preferred embodiment” as a rationale to depart from the plain meaning of “said signal converters.” The Board’s decision and underlying analyses was flawed because the specification makes the point that processing dither signal through all the stages is how the system linearity is improved and the goal of the invention achieved. The Board conceded as much. Appx16 (“we understand from *a plain reading of the ’452 patent*, that ‘using fewer than all the digital codes output by all the signal converters would result in digital output of the converter that does not correctly reflect the input analog signal.’”) (emphasis added). Simply put, the

specification makes clear what the invention is *not*: Figure 7A. Appx27. And what the invention is: Figures 7B and 7C. Appx28. The Board’s findings on the ’452 patent’s disclosure in relation to interpreting the claims should be discarded. This Court should reverse the Board’s holding and construe the claims to mean all signal converters process the signals.

E. None of the prior art references disclose processing the dither signals and samples by all the signal converters.

As noted above, independent claims 1 and 13 were challenged on two grounds: (1) single-reference obviousness based on Cesura, and (2) a combination of Fu and Lewis. Appx17. None of the references, however, discloses a dither signal and samples “processed along different signal-processing paths of said signal converters,” as claimed. Appx83 at 16:16-18; Appx84 at 17:26-28.

Indeed, for both grounds of challenge, the Board did not find that any reference discloses that a dither signal is processed through *all* the signal converters. Instead, for both grounds, Xilinx argued that the dither signal will be processed by *at least one* stage of the pipelined ADC. *See, e.g.*, Appx181 (“Cesura’s analog dither signals [t] will cause *at least one stage* of its pipelined ADC to operate at different operating points, depending on the value of the dither signal at any given moment.”); Appx920 at ¶106; Appx226-227 (“Fu’s analog dither signals will cause *at least one stage* of its pipelined ADC to operate at

different operating points, depending on the value of the dither signal at any given moment.”); Appx984-985 at ¶200 (emphases added). But, as shown above, “said signal converters” means “*all* said signal converters” and not “*at least one* stage.”

In its analysis with respect to Cesura (Ground A), the Board relied heavily on the testimony of Xilinx’s expert, Dr. Holberg. Appx30-35. But even Xilinx’s expert did not proffer that Cesura’s test signal is processed by *all* the signal converters. Instead, Xilinx’s expert agreed that Figure 2 of Cesura *does not* disclose signals being processed by any of the successive signal converters:

Q. So in Figure 2, Stages 105/20 represent Stages 105/2, 105/1, and 105/0, shown in the prior art Figure 1, correct?

A. Correct.

Q. And so Figure 2 does not represent an embodiment where the correction circuitry is applied to Stages 105/2, 105/1, or 105/0, correct?

A. *[T]his figure doesn’t.*

Appx31 (emphasis added).

The Board, however, held that “that although Figure 2 [of Cesura], which is a circuit diagram, does not show specific processing being carried out by subsequent stages,” a POSITA could understand the signals may be processed by one or more stages because Dr. Holberg testified that “the algorithm *could apply* to *one or more stages, that maybe it does.*” Appx32-33 (emphasis added). The mere

possibility that Cesura's test signal (t) could "maybe" apply to "*one or more stages*" is not the same as disclosure that the test signal that is processed by *all* the stages (i.e., signal converters). Indeed, Dr. Holberg testified that even if at least one successive stage processes the test signal, none of the subsequent stages after that in the system process the test signal:

Q. So looking at Figure 2 of Cesura, can you come to any certain conclusion regarding whether Stage 105/1 randomizes its signal-processing paths based on the test signal t input into Stage 105/3?

A. Yeah, like I said a while ago, I can't say for certain. I – I'm pretty confident that the next stage does, 105/2. But the – *the following two stages may well not.*

Appx1711 at 91:23-92:10 (emphasis added).

Simply put, Xilinx's own expert conceded that Cesura does not disclose that *all* signal converters process a dither signal and, at best, one or more stages "could" or "maybe" process it. But relying on a flawed claim construction, the Board simply held that "[w]e are persuaded by the arguments and evidence of record that a person of ordinary skill in the art would have understood that Cesura's test signal t is applied to *multiple* stages of the signal converter system." Appx34 (emphasis added). Multiple stages and *all* stages are not synonymous, and thus the Board erred.

And for Ground C (Fu and Lewis combination), the Board similarly held that the claims do not require the signal to be processed along different signal-processing paths “of *each* of the *multiple* signal converters in the analog-to-digital converter,” and therefore the lack of the disclosure by prior art of signal processed by all signal converters was not fatal. Appx53 (emphasis in original). The Board’s analysis here, too, was flawed and contrary to the evidence presented.

The Fu article discusses using multiple ADCs by “time interleaving” the ADCs in order to achieve a faster sampling rate than you would get with just one ADC. Appx1650 at ¶85. But Fu is silent regarding injecting dither such that it is processed through each stage. Neither the Board nor Xilinx point to where or how Fu show such a feature. As noted above, Xilinx simply argued that the dither signal will be processed by *at least one* stage of the pipelined ADC. Appx226-227 (“Fu’s analog dither signals will cause *at least one stage* of its pipelined ADC to operate at different operating points, depending on the value of the dither signal at any given moment.”); Appx984-985 at ¶200 (emphases added). And Xilinx’s expert did not analyze the issue at all in forming his opinion:

Q. Did you analyze how any of Stages 2 through 13 responds to the random signal input into the pipeline [of Fu]?

A. . . . I didn’t try to figure out how far – how many stages down before it didn’t or if it ever - it may have done – it may do it on all stages

Appx1721 at 132:4-24.

Thus, the Board did not find that Fu (or Lewis) teaches a POSITA that dither should be processed through all the signal converters. The Board, again, leaned heavily on its claim construction to suggest that such evidence was not needed because “said signal converters” does not mean “all said signal converters.”

Appx53.

Because substantial evidence is not present for the Board’s finding of obvious of the combination of Fu and Lewis, the Board’s holding should be reversed.

CONCLUSION AND RELIEF SOUGHT

Analog requests that this Court vacate the Board’s erroneous claim construction, hold that the claim language requires processing through all of the signal converters, and reverse the Board’s findings that the claims are obvious.

Dated: November 3, 2022

Respectfully submitted,

/s/ Janine A. Carlan

Janine A. Carlan
Taniel Anderson
Jasjit S. Vidwan
ArentFox Schiff LLP
1717 K Street, NW
Washington, DC 20006
202.857.6000
janine.carlan@afslaw.com

*Counsel for Appellant,
Analog Devices, Inc.*

ADDENDUM

TABLE OF CONTENTS

	Page(s)
Final Written Decision, IPR2020-01561	Appx1-63
U.S. Patent No. 7,719,452.....	Appx64-84

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

XILINX, INC. and XILINX ASIA PACIFIC PTE. LTD.,
Petitioner,

v.

ANALOG DEVICES, INC.,
Patent Owner.

IPR2020-01561
Patent 7,719,452 B2

Before JEFFREY S. SMITH, SCOTT A. DANIELS, and
GEORGIANNA W. BRADEN, *Administrative Patent Judges*.

DANIELS, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining All Challenged Claims Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

A. *Background*

On September 1, 2020, Xilinx, Inc. and Xilinx Asia Pacific Pte. Ltd. (collectively, “Petitioner”) filed a Petition requesting an *inter partes* review of claims 1–4, 8, 9, 12–16, 19, and 20 of U.S. Patent No. 7,719,452 B2, issued on May 18, 2010 (Ex. 1001, “the ’452 patent”). Paper 1 (“Pet.”). Analog Devices, Inc. (“Patent Owner”) filed a Preliminary Response. Paper 7 (“Prelim. Resp.”).

Following our Institution Decision (Paper 10, “Inst. Dec.”), Patent Owner filed a Response. Paper 13 (“PO Resp.”). Petitioner filed a Reply. Paper 19 (“Reply”). Patent Owner filed a Sur-Reply. Paper 20 (“PO Sur-Reply”). A hearing was held on December 9, 2021. A transcript of the hearing has been entered as Paper 26 (“Tr.”).

We have jurisdiction under 35 U.S.C. § 6. This Final Written Decision is entered pursuant to 35 U.S.C. § 318(a). We determine that claims 1–4, 8, 9, 12–16, 19 and 20 are unpatentable.

B. *Additional Proceedings*

The parties indicate that the ’452 patent has been asserted against Petitioner in *Analogy Devices, Inc. v. Xilinx, Inc. and Xilinx Asia Pacific Pte. Ltd.*, Case No. 1:19-cv-02225 in the United States District Court for the District of Delaware. Pet. 97; Paper 5, 2. Patent Owner also states that “Petitioner[] filed petitions for *Inter Partes* Review of U.S. Patent No. 10,250,250 (Case No. IPR2020-01210), U.S. Patent No. 8,487,659 (Case No. IPR2020-01219), U.S. Patent No. 7,012,463 (Case No. IPR2020-01336), U.S. Patent No. 7,286,075 (Case No. IPR2020-01559), and U.S. Patent No. 6,900,750 (Case Nos. IPR2020-01483, IPR2020-01484, and IPR2020-01564), which are also at issue in the above litigation.” Paper 5, 2.

C. Real Parties in Interest

The Petition identifies Xilinx, Inc. and Xilinx Asia Pacific Pte. Ltd. as Real Parties in Interest. Pet. 97. Patent Owner identifies itself as the Real Party in Interest. Paper 5, 2.

D. The '452 Patent (Ex. 1001)

The '452 patent describes analog to digital converter (ADC) systems that convert analog signals to digital signals. Ex. 1001, 1:10–12. More specifically, the '452 describes a “pipelined” or “cascade” signal converter that uses lower resolution converter stages to achieve higher signal resolution at greater sampling speeds. *Id.* at 1:12–16. The '452 patent explains that

[e]ach stage of a pipelined system quantizes that stage’s input signal to a predetermined number of digital bits and forms an analog output signal which is presented to a succeeding stage for further signal processing.

Id. at 1:16–19. Figure 1 of the '452 patent, reproduced below, illustrates an embodiment of such a pipelined ADC system.

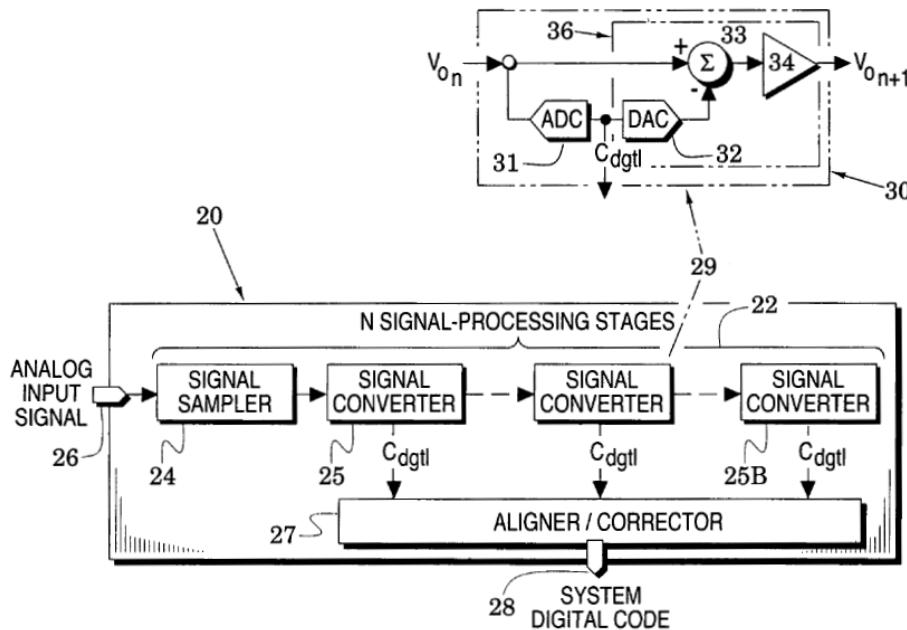


FIG. 1

IPR2020-01561
Patent 7,719,452 B2

Figure 1 of the '452 patent, reproduced above, illustrates a block-diagram of a pipelined ADC system including analog input signal 26, signal sampler 24, N signal processing stages 25[N], alignor/corrector 27 and system digital code output 28. A circuit diagram, Figure 2, reproduced below, illustrates an exemplary signal converter circuit structure according to the '452 patent. *Id.* at 3:32–34.

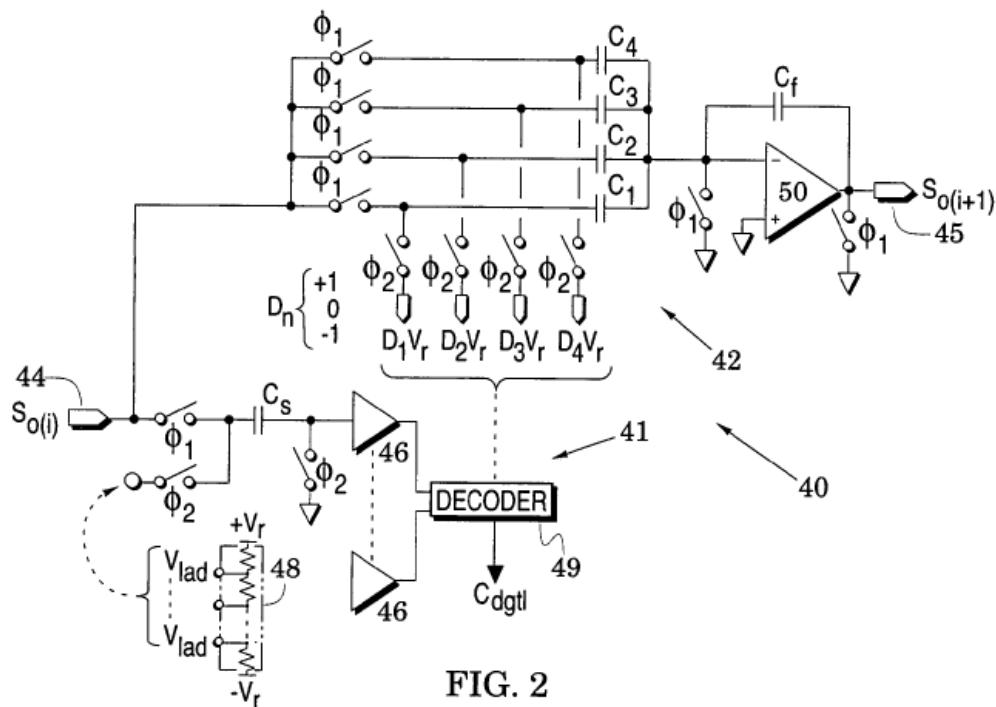


FIG. 2

Figure 2 of the '452 patent, above, shows an embodiment of signal converter 40 including a multiplying digital-to-analog converter 42 (MDAC) and switched-capacitor signal comparator 41. *Id.* at 3:40–42.

The '452 patent further describes a problem with such systems where “converter nonlinearity” between the stages of a pipelined signal converter “can significantly degrade the conversion of low-level dynamic signals.” *Id.* at 1:25–26. A goal of the ADC system described in the '452 patent is to provide “pipelined converter systems with enhanced linearity.” *Id.* at 1:51–

IPR2020-01561
Patent 7,719,452 B2

52. The '452 patent explains that better linearity addresses the problem where

the signal converter 40 of FIG. 2 will introduce undesirable symmetrical INL [integral nonlinearity] errors (e.g., as exemplified by segments 74 of the INL 70) into the transfer function of the converter system 20 of FIG. 1. Although these symmetrical transfer function errors have been described above to originate from incorrect feedback capacitor C_f size and insufficient amplifier gain, they can also originate from other system errors (e.g., signal setting errors).

Id. at 5:49–56. To account for these, and other such errors, the '452 patent describes the addition of pseudo-random (PN) generator 81, and also PN generator 85, to system 20, as illustrated in Figure 6 reproduced below.

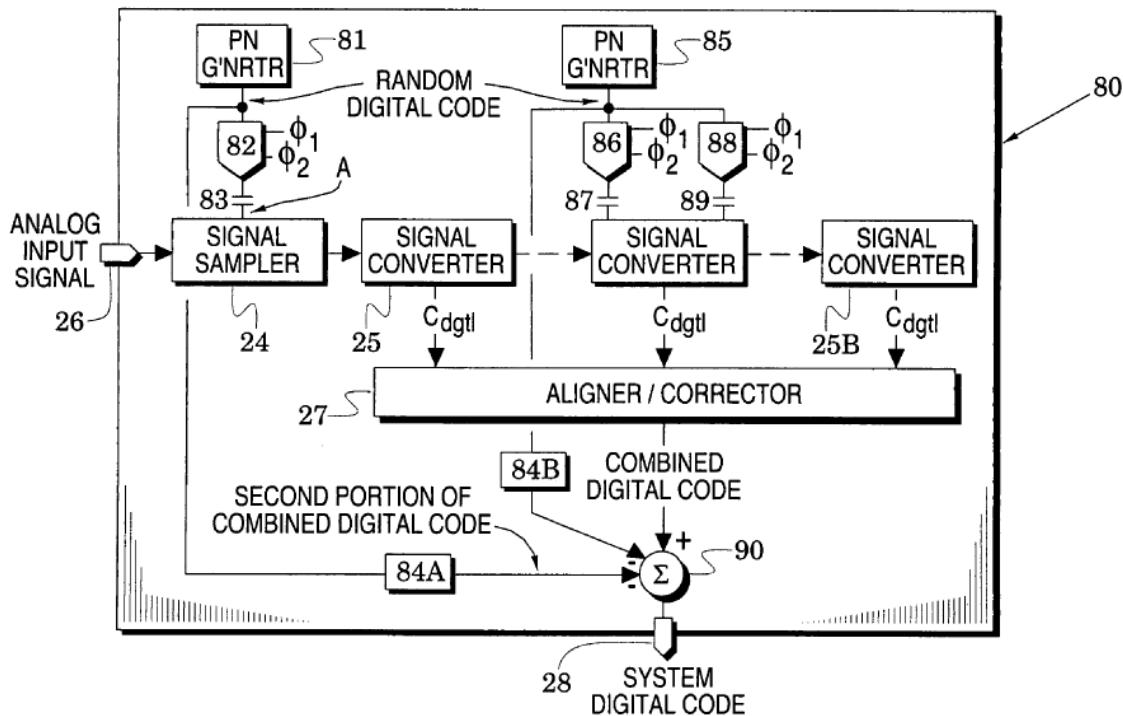


FIG. 6

Figure 6 of the '452 patent, above, shows PN generator 81, digital analog converter (DAC) 82, and dither capacitor 83 for injecting analog dither

IPR2020-01561
Patent 7,719,452 B2

signals into signal sampler 24. According to the '452 patent, the analog dither signals and analog input to signal sampler 24 are combined and the combined signal is processed down randomly-selected signal-processing paths of the converter system which induce different magnitudes and signs of INL errors. The average error of these processing paths is reduced to thereby provide significant improvements in system linearity . . . these linearity improvements are realized by simultaneous processing of two combined analog signals—the input signal at the input port 26 and the injected dither signal.

Id. at 6:17–26. The '452 patent explains further that

[a]s shown in FIG. 6, this processing provides a combined digital code at the output of the aligner/corrector 27. A first portion of this combined digital code at the digital back-end of the signal converter corresponds to the analog input signal that was earlier received into the input port 26 but a second portion of the combined digital code corresponds to the injected analog dither signal. In the converter system 80, the final system digital code at the output port 28 is realized by subtracting out the second portion in a differencer 90.

Id. at 6:26–35.

The '452 patent also describes that a similar ADC signal resolution process can occur for downstream signal converter 25, also shown in Figure 6, having PN generator 85, DAC 86, 88, and respective dither capacitors 87, 89 providing analog dither signals for combination with the input analog signal. *Id.* at 6:44–67.

E. Illustrative Claim

Of the challenged claims, claims 1 and 13 are independent. Each of dependent claims 2–4, 8, 9, and 12 depend from claim 1, and claims 14–16, 19, and 20 depend from claim 13. Claim 1 illustrates the claimed subject matter and is reproduced below with certain limitations of interest highlighted in italics (bracketed limitation numbering added):

IPR2020-01561
Patent 7,719,452 B2

1. [1A] An analog-to-digital converter system to convert an analog input signal to a system digital code, comprising:
 - [1B] a sampler to provide samples of said analog input signal;
 - [1C] signal converters arranged and configured to successively process said samples;
 - [1D] at least one digital-to-analog converter configured to respond to a random digital code *and inject analog dither signals into at least a selected one of said sampler and said signal converters* which process said samples and said analog dither signals into a plurality of digital codes;
 - [1E] an aligner/corrector coupled to said signal converters to process said plurality of digital codes into a combined digital code that includes a first portion that corresponds to said samples and a second portion that corresponds to said analog dither signals; and
 - [1F] a decoder having a transfer function configured to convert said random digital code to said second portion for differencing with said combined digital code to thereby provide said system digital code;
 - [1G] *said samples thus processed along different signal-processing paths of said signal converters to thereby enhance linearity of said system.*

Ex. 1001, 15:63–16:18 (emphasis added).

F. Level of Ordinary Skill in the Art

Factors pertinent to a determination of the level of ordinary skill in the art include: (1) educational level of the inventor; (2) type of problems encountered in the art; (3) prior art solutions to those problems; (4) rapidity with which innovations are made; (5) sophistication of the technology, and (6) educational level of workers active in the field. *Env'tl. Designs, Ltd. v. Union Oil Co.*, 713 F.2d 693, 696–697 (Fed. Cir. 1983) (citing *Orthopedic Equip. Co. v. All Orthopedic Appliances, Inc.*, 707 F.2d 1376, 1381–82 (Fed. Cir. 1983)). Not all such factors may be present in every case, and one or more of these or other factors may predominate in a particular case.

IPR2020-01561
Patent 7,719,452 B2

Id. Moreover, these factors are not exhaustive but are merely a guide to determining the level of ordinary skill in the art. *Daiichi Sankyo Co. Ltd, Inc. v. Apotex, Inc.*, 501 F.3d 1254, 1256 (Fed. Cir. 2007).

In determining a level of ordinary skill, we also may look to the prior art, which may reflect an appropriate skill level. *Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001). Additionally, the Supreme Court informs us that “[a] person of ordinary skill is also a person of ordinary creativity, not an automaton.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 421.

Petitioner, supported by the testimony of Dr. Holberg, proposes that a person of ordinary skill in the art (“POSITA”):

would have at least a Master’s Degree in Electrical Engineering or equivalent field, including studies in the area of analog circuitry, or at least a Bachelor’s Degree in Electrical Engineering and two years of experience working on analog circuitry design.

Pet. 16–17 (citing Ex. 1002 ¶¶ 16–19).

Patent Owner’s declarant, Dr. Moon states that Petitioner’s asserted level of ordinary skill in the art is “reasonable.” Ex 2002 ¶ 13.

Petitioner’s proposed level of ordinary skill in the art is consistent with our review and understanding of the technology and descriptions in the ’452 patent and the prior art references that disclose electronic circuits including pipelined analog-to-digital converters and discussion of the nonlinearity problems due to offset, gain, and aperture mismatches in analog to digital signal conversion. And, because the parties generally agree, we apply Petitioner’s proposed level of ordinary skill in the art.

G. Claim Construction

We interpret claims in the same manner used in a civil action under 35 U.S.C. § 282(b) “including construing the claim in accordance with the

IPR2020-01561
Patent 7,719,452 B2

ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.” *See Changes to the Claim Construction Standard for Interpreting Claims in Trial Proceedings Before the Patent Trial and Appeal Board*, 83 Fed. Reg. 51,340, 51,358 (Oct. 11, 2018) (amending 37 C.F.R. §42.100(b) effective November 13, 2018) (now codified at 37 C.F.R. § 42.100(b) (2020)).¹ Only terms that are in controversy need to be construed, and then only to the extent necessary to resolve the controversy. *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017).

Petitioner relies on the opinion testimony of Dr. Douglas R. Holberg (Ex. 1002). Patent Owner’s arguments are supported by the testimony of Dr. Un-Ku Moon (Ex. 2002).

“*said signal converters*”

Claim limitations 1[B]–[D] and [G] recite:

[1B] a sampler to provide samples of said analog input signal;

[1C] signal converters arranged and configured to successively process said samples;

[1D] at least one digital-to-analog converter configured to respond to a random digital code and inject analog dither signals into *at least a selected one of said sampler and said signal converters* which process said samples and said analog dither signals into a plurality of digital codes

...

[1G] said samples thus processed along different signal-processing paths of *said signal converters* to thereby enhance linearity of said system.

¹ This rule change applies to the instant Petition because it was filed after November 13, 2018. *See id.*

IPR2020-01561
Patent 7,719,452 B2

Ex. 1001, 15:65–16:6.

We determined in our Institution Decision that claim 1 “only requires that samples be processed along different signal-processing paths of *at least one* stage of the pipelined converter.” Inst. Dec. 24. In this Decision, based on the parties’ arguments and evidence, and for the reasons explained below, we clarify our claim construction.

Patent Owner argues that claim 1[C] “recites that the conversion is performed by a series of ‘signal converters’ arranged and configured to ‘successively process’ samples of the analog input signal into a ‘plurality of digital codes.’” PO Resp. 25. Patent Owner argues that each of the signal converters is “a different *stage* in the pipelined converter system.” *Id.* at 26 (citing Ex. 1001, 1:10–19, 2:48–57, Fig. 1; Ex. 2002 ¶ 54). Patent Owner then asserts for claim 1[D] “that dither is injected into the sampler or the signal converters.” *Id.* In this way, Patent Owner argues for claim limitation 1[G] that “the injected dither propagates through *all* of the stages, causing the samples to be processed along different signal-processing paths of all of the converter stages.” *Id.* at 26–27.

Patent Owner contends that the Specification of the ’452 patent supports their construction. PO Resp. 29–34. Patent Owner argues specifically that as shown by comparing Figures 7A and 7B, the ’452 patent confirms that, compared to known systems, the novelty of the claims lies in “propagation of dither through *all* stages of the converter system.” *Id.* at 31 (citing Ex. 1001, 8:53–56, 10:65–67, 11:59–65, 14:5–9, 39–55). Figure 7A illustrates one embodiment where only some of the signal converters, i.e., stages 1 and 2, process the respective combined signal (101–102) at different operating points, while Figure 7B illustrates another embodiment where all

IPR2020-01561
Patent 7,719,452 B2

stages 1–5 processes the combined signal (101–105) at different operating points. *Id.*

Patent Owner also relies on Dr. Moon’s testimony that “in the context of the patent specification and claims, the phrase ‘said signal converters’ in limitations [1G] and [13F] . . . refers back to the multiple ‘signal converters arranged and configured to successively process samples’ in limitation [1C] and [13B].” *Id.* at 36–36 (citing Ex. 2002 ¶ 54). Dr. Moon surmises that

a POSITA would have understood the reference to “said signal converters” in limitations [1C] and [13B] to refer to all the signal converters in an ADC pipeline, because each of them generates a different digital code reflecting a different portion of the input analog signal. Using fewer than all the digital codes output by all the signal converters would result in digital output of the converter that does not correctly reflect the input analog signal.

Ex. 2002 ¶ 55.

In sum, the argument presented by Patent Owner is that independent claims 1 and 13 recite, structurally, a plurality, or multiple “signal converters,” and therefore functionally require, “that the input samples be processed along different signal-processing paths in *each* of the *multiple* stages of the converter system.” *Id.* at 25.

We agree that “said signal converters” in claim 1[G] is plural and the antecedent basis is found in the recitation of “signal converters” in claim limitation 1[C]. Ex. 1001, 15:66–16:17. What we are not persuaded by is Patent Owner’s arguments and evidence that limitation 1[G] should be read as “*all* said signal converters.”

As an initial matter, on its face, claim 1[G] does not recite “*all*,” or “*each of*” said signal converters. Given a plain reading of the claim, we are not apprised that the language, on its face, limits the claim to processing the combined input and dither sample “along different signal-processing paths

IPR2020-01561
Patent 7,719,452 B2

of [all] *said signal converters*.” We acknowledge that there is proper antecedent basis in the claim 1[C] for “said signal converters,” but Patent Owner has not explained persuasively how merely having successive pipelined signal converters extends to the functional requirement of signal samples being “processed along different signal-processing paths of [all] said signal converters.” Indeed, as Patent Owner points out, the Specification explains that “[i]n a feature of the present disclosure, however, dither points propagate through the converter stages and cover a substantial portion of *each converter subrange as shown in FIG. 7B*.” PO Resp. 20–21 (citing Ex. 1001, 14:39–52; Ex. 2002 ¶ 50). Because this feature, or embodiment, of the invention was clearly discussed in the Specification of the ’452 patent, it would have been an elementary matter for the claim to have been similarly drafted to specify this limitation, e.g., by writing the limitation as “*all* said signal converters,” or alternatively “*each of* said signal converters.” This, however, is not the case.

The Specification of the ’452 patent provides a description of the figures, including:

FIG. 6 is a diagram of a converter system embodiment of the present disclosure;

FIG. 7A illustrate transfer functions of signal-processing stages in the system of FIG. 6 and possible dither levels in these stages;

FIG. 7B is similar to FIG. 7A and illustrates preferred dither levels;

Ex. 1001, 2:1–7. Thus, in the disclosed embodiment of Figure 6, the converter system embodiment can provide “possible dither levels” as shown in Figure 7A, or “preferred dither levels,” as shown in Figure 7B. Figures 7A and 7B are reproduced below.

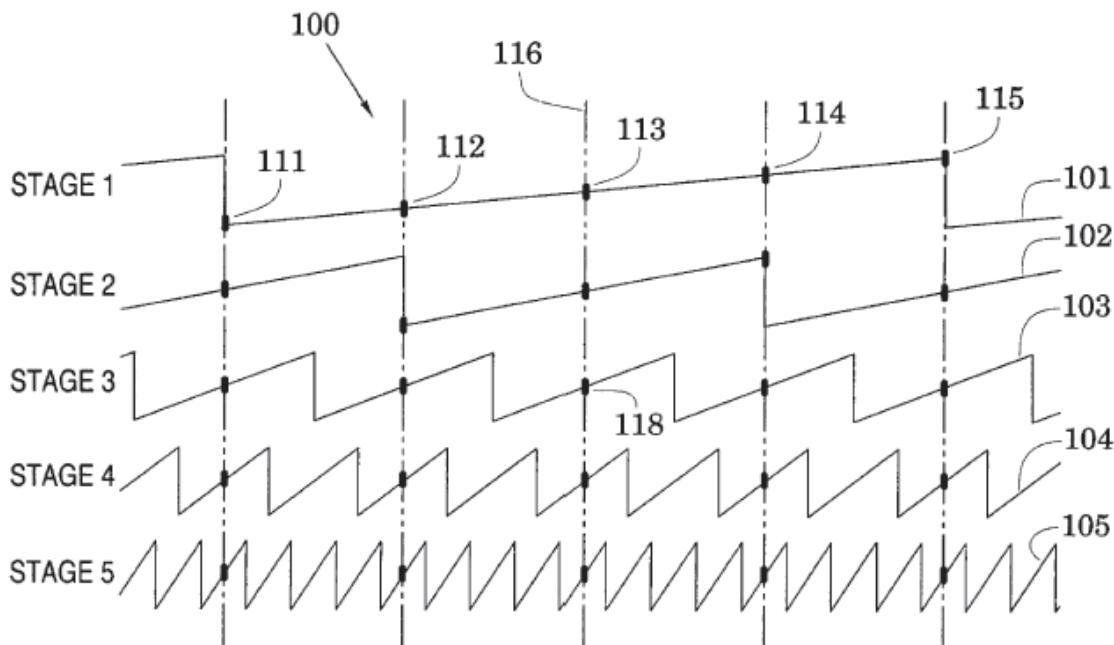


FIG. 7A

Figure 7A, above, illustrates one embodiment of the converter system in Figure 6 where stages 1 and 2 process the respective combined signal (101–102) at different operating points. But, in each of stages 3–5, the signal is processed at the same operating points. *See id.* at 7:52–56 (The written description explaining that “the operating point in subsequent stages 3–5 remains at the operating point prior to application of dither.”).

IPR2020-01561
Patent 7,719,452 B2

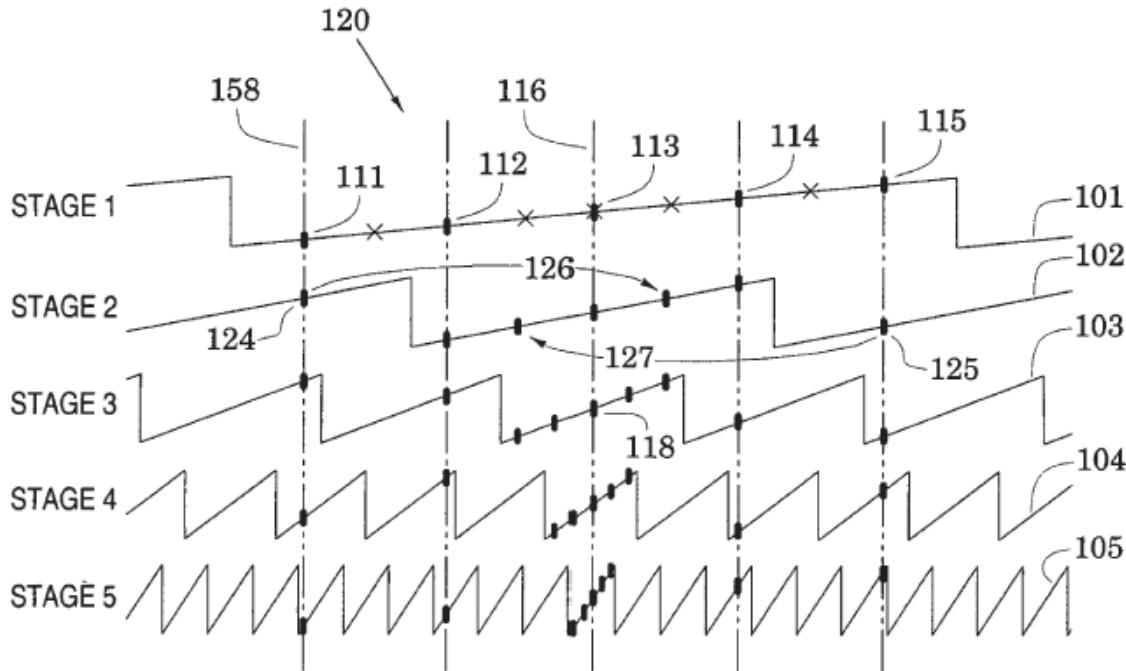


FIG. 7B

Figure 7B, above, illustrates, compared to Figure 7A, a preferred result of the converter system illustrated in Figure 6 where each stage 1–5 processes the combined signal (101–105) at different operating points. Patent Owner asserts that the difference between Figures 7A and 7B illustrates the problem of “dither exhaustion.” PO Resp. 10.

Because both Figures 7A and 7B are embodiments of the signal converting structure shown in Figure 6, we appreciate that Figure 7B shows a preferable result where the processing of the input signal along more stages having different signal processing paths helps improve the system linearity and achieve a more accurate signal conversion result. Yet we do not read the Specification and the embodiments of Figures 6, 7A, and 7B as being such disparate embodiments that they cannot be covered by the claim language or, that the comparison is somehow a disavowal of claim scope. We acknowledge that the Specification discusses the embodiment of Figure

IPR2020-01561
Patent 7,719,452 B2

7B, having more processing paths, being the most preferred. *See, e.g., id.* at 10:65–67 (“The different operating points in FIG. 7B illustrate the processing advantages of dither structure embodiments of the present disclosure.”). We would agree that Figure 7A is mainly described as a less preferred embodiment of the converter system shown in Figure 6 where “dither exhaustion” may occur. Yet, the ’452 patent does not describe Figure 7A as representative of the prior art or distinguish it in a way other than to be less preferred than Figure 7B. Overall, the Specification mainly describes that the embodiment of Figure 7B is preferred over that of Figure 7A, and does not specify any persuasive description or statements limiting “signal converters” to meaning “*all* signal converters” in the context of processing the combined input and dither sample “along different signal-processing paths of *said signal converters*,” as recited in claim 1. We also do not find a disavowal of the embodiment in Figure 7A because disavowal of claim scope generally requires an express disavowal or disclaimer. *See Retractable Techs., Inc. v. Becton, Dickinson & Co.*, 653 F.3d 1296, 1306 (Fed. Cir. 2011) (The Federal Circuit explaining that “[t]o disavow claim scope, the specification must contain ‘expressions of manifest exclusion or restriction, representing a clear disavowal of claim scope.’”)
(quoting *Epistar Corp. v. Int'l Trade Comm'n*, 566 F.3d 1321, 1335 (Fed. Cir. 2009)).

Patent Owner further contends that during prosecution of the application which became the ’452 patent “[i]n the Notice of Allowance, the Examiner specifically referred to the ‘different signal-processing paths in said signal converters’ limitation as being one of the novel features in the claims.” PO Resp. 24 (citing Ex. 1003, 165–166). The Examiner’s reasons for allowance stated that “prior art considered individual or combination

IPR2020-01561
Patent 7,719,452 B2

does not teach an analog-to-digital converter system comprising,” and then essentially copied claim limitations 1[E]–[G], and similarly claim limitations 13[E]–[G], as the noted reasons for allowance. Ex. 1003, 165–166. The Examiner’s reasons for allowance did not indicate in any express way that “said signal converters” was interpreted as “[all] said signal converters,” or “[each of] said signal converter.” *Id.*

Dr. Moon’s testimony does not persuasively support Patent Owner’s construction because it mainly reiterates what we understand from a plain reading of the ’452 patent, that “[u]sing fewer than all the digital codes output by all the signal converters would result in digital output of the converter that does not correctly reflect the input analog signal.” Ex. 2002 ¶ 55. In other words, the more signal converters that operate over different operating points, the better. Overall, Dr. Moon’s testimony is consistent with our understanding from reading the Specification, that the embodiment of Figure 7B is better and preferred because it would result in a more accurate signal conversion than the Figure 7A embodiment. In our view, even considering the issue of “dither exhaustion” which is not expressly recited in the ’452 patent, Patent Owner has not pointed to persuasive evidence either in the claims, Specification, prosecution history, or Dr. Moon’s testimony as to why a person of ordinary skill in the art would read the claim language as excluding the embodiment in Figure 7A or, that the ’452 patent expressly disavows embodiments which alter the signal processing paths in less than all the signal converters.

We find that Patent Owner’s construction depends improperly on reading limitations, namely that dither propagates through *all* the converter stages, from the Specification into the claims. *See* PO Resp. 31, *see also* *Hill-Rom Servs., Inc. v. Stryker Corp.*, 755 F.3d 1367, 1371 (Fed. Cir. 2014)

IPR2020-01561
Patent 7,719,452 B2

(The Federal Circuit explaining that “[w]hile we read claims in view of the specification, of which they are a part, we do not read limitations from the embodiments in the specification into the claims.”). Accordingly, we alter our claim construction from our Institution Decision, and determine that for limitations 1[G] and 13[F], “said samples thus processed along different signal-processing paths of *said signal converters* to thereby enhance linearity of said system,” is not limited to, or properly interpreted as, processing samples along “*all* said signal converters” in the claimed analog-to-digital converter systems.

H. Grounds Asserted

Petitioner asserts that the challenged claims are unpatentable on the following grounds:

Claims Challenged	35 U.S.C. §	Reference(s)/Basis
1, 2, 8, 9, 13–16	103(a)	Cesura ²
12, 19, 20	103(a)	Cesura, Lewis, ³ and Bjornsen ⁴
1–4, 8, 9, 13–16	103(a)	Fu ⁵ and Lewis
12, 19, 20	103(a)	Fu, Lewis, and Bjornsen

II. ANALYSIS

A. Legal Standards of Obviousness

Section 103(a) forbids issuance of a patent when “the differences between the subject matter sought to be patented and the prior art are such

² Ex. 1004, US Patent No. 6,970,125 B2 (Nov. 29, 2005).

³ Ex. 1006, Stephen H. Lewis and Paul R. Gray, “A Pipelined 5-Msample/s 9-bit Analog-to-Digital Converter,” *IEEE Journal of Solid State Circuits*, Vol. SC-22, No. 6, Dec. 1987.

⁴ Ex. 1007, US Patent No. 7,129,874 B2 (Oct. 31, 2006).

⁵ Ex. 1005, Daihong Fu et al., “A Digital Background Calibration Technique for Time-Interleaved Analog-to-Digital Converters,” *IEEE Journal of Solid State Circuits*, Vol. 33, No. 12, Dec. 1998.

IPR2020-01561
Patent 7,719,452 B2

that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.” *KSR*, 550 U.S. at 406.

The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) when available, objective evidence such as commercial success, long-felt but unsolved needs, and failure of others. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966); *see KSR*, 550 U.S. at 407 (“While the sequence of these questions might be reordered in any particular case, the [*Graham*] factors continue to define the inquiry that controls.”). The Court in *Graham* explained that these factual inquiries promote “uniformity and definiteness,” for “[w]hat is obvious is not a question upon which there is likely to be uniformity of thought in every given factual context.” *Graham*, 383 U.S. at 18.

The Supreme Court made clear that we apply “an expansive and flexible approach” to the question of obviousness. *KSR*, 550 U.S. at 415. Whether a patent claiming the combination of prior art elements would have been obvious is determined by whether the improvement is more than the predictable use of prior art elements according to their established functions. *Id.* at 417. To reach this conclusion, however, it is not enough to show merely that the prior art includes separate references covering each separate limitation in a challenged claim. *Unigene Labs., Inc. v. Apotex, Inc.*, 655 F.3d 1352, 1360 (Fed. Cir. 2011). Rather, obviousness additionally requires that a person of ordinary skill at the time of the invention “would have selected and combined those prior art elements in the normal course of research and development to yield the claimed invention.” *Id.*

IPR2020-01561
Patent 7,719,452 B2

A claimed invention may be obvious even when the prior art does not teach each claim limitation, so long as the record contains some reason why one of skill in the art would have modified the prior art to obtain the claimed invention. *See Ormco Corp. v. Align Tech., Inc.*, 463 F.3d 1299, 1307 (Fed. Cir. 2006). And, as a factfinder, we also must be aware “of the distortion caused by hindsight bias and must be cautious of arguments reliant upon *ex post* reasoning.” *KSR*, 550 U.S. at 421. This does not deny us, however, “recourse to common sense” or to that which the prior art teaches. *Id.*

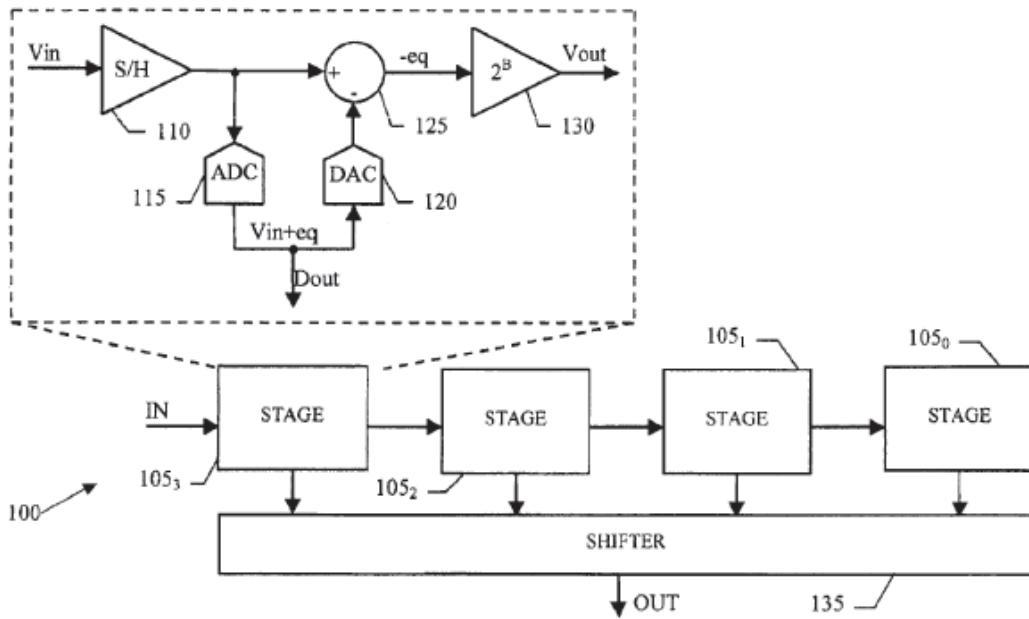
B. Obviousness over Cesura, claims 1, 2, 8, 9, 13–16

Petitioner argues that claims 1, 2, 8, 9, and 13–16 of the '452 patent would have been obvious over Cesura. As discussed below, and having reviewed the full record now before us, including the relevant portions of the supporting testimony of Dr. Holberg and Dr. Moon we are persuaded that Petitioner has demonstrated by a preponderance of the evidence that the challenged claims would have been unpatentable over Cesura.

1. Overview of Cesura (Ex. 1012)

Cesura discloses a pipelined ADC system shown for example in Figure 1, reproduced below, labeled “Prior Art,” where ADC system 100 includes pipelined converter stages 105₃–105₀ for successively processing the sampled analog signal IN. Ex. 1004, 2:61–67.

IPR2020-01561
Patent 7,719,452 B2



*FIG. 1
(Prior Art)*

Cesura's Figure 1, above, schematically illustrates a pipeline ADC system including that converter stages 105₃–105₀ determine respective analog outputs Dout that are combined and processed by shifter 135 into digital output signal OUT. *Id.*

Figure 2 of Cesura, reproduced below, reveals a schematic of an embodiment of an ADC converter.

IPR2020-01561
Patent 7,719,452 B2

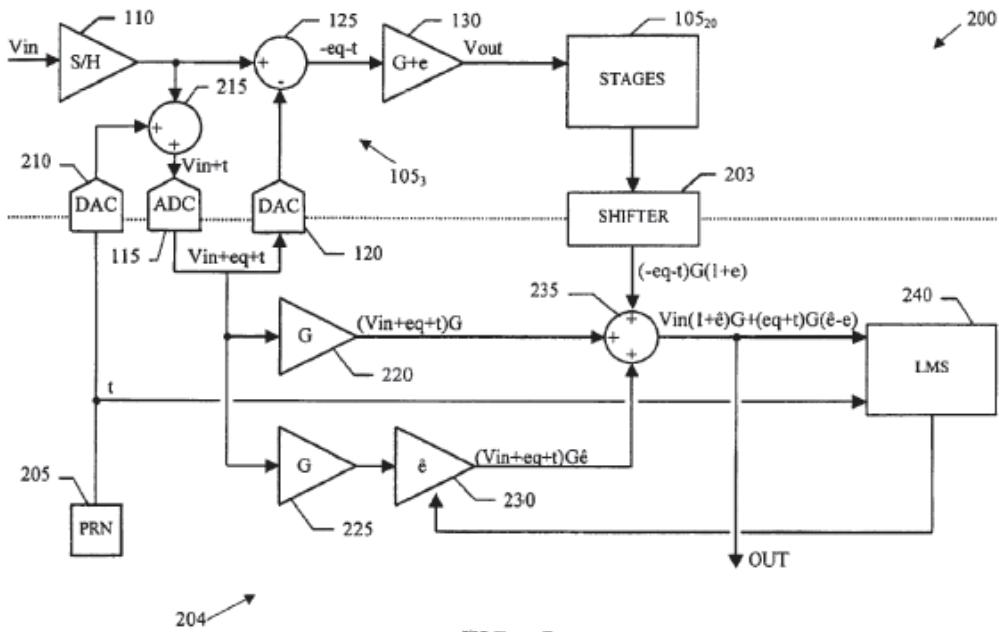


FIG. 2

Cesura's Figure 2, above, illustrates an embodiment of pipelined ADC converter 200 including pseudo-random noise (PRN) generator 205 that provides via DAC 210, a test analog signal t that is combined in adder 215 with analog input signal V_{in} , from sampler 110. *Id.* at 4:8–14. Adder 215 thus provides through amplifier 130 analog V_{out} that is a combination of test analog signal t and the sampled analog V_{in} input signal. *Id.* at 4:12–18.

In the embodiment of Figure 2, stages 105_{20} produce digital output signals and shifter 203 combines these digital output signals into a combined digital output signal that is sent to adder 235. *Id.* at 4:23–33. Cesura states that “[t]he digital signal $V_{in}(1+e)G+(eq+t)G(e-e)$ from the adder 235 represents the digital output signal OUT of the whole converter 200.” *Id.* at 4:55–57. In conjunction with adder 235, logic module 240 receives the digital test signal directly from PN generator 25 and Cesura states that “the additive term (including the digital test signal t) due to the analog error e of the amplifier 130 providing the inter-stage gain is deleted.” *Id.* at 4:59–61. Cesura explains that “[t]he solution of the invention substantially reduces the

IPR2020-01561
Patent 7,719,452 B2

distortion (in the digital signal generated by the converter) caused by the analog error in the inter-stage gain.” *Id.* at 6:30–33.

2. *Independent Claims 1 and 13*

Considering elements [1A]-[1G] of claim 1, as reproduced above, and independent claim 13, we address below the respective arguments of both parties as to claim 1.

a) *Petitioner’s Arguments*

(1) *Preamble [1A]*

Petitioner argues that to the extent the preamble is limiting, “Cesura discloses in Figure 2, [] a pipelined analog-to-digital converter 200 that converts analog input signal ‘Vin’ [] into a corresponding digital output code ‘OUT.’” Pet. 17 (citing Ex. 1002 ¶¶ 92–93).

(2) *Limitation [1B]*

Relying on Dr. Holberg’s testimony, Petitioner argues that Cesura’s ADC system 200 includes “sample/hold (S/H) amplifier 110” that samples the input signal Vin and provides the sampled signal to flash ADC 115. Pet. 18 (citing Ex. 1002 ¶ 94).

(3) *Limitation [1C]*

With respect to “signal converters arranged and configured to successively process said samples,” Petitioner argues that Cesura’s signal converters 105₃–105₀ are arranged and configured to successively process the sample input signal. Pet. 18. Dr. Holberg testifies that this is demonstrated “by the input signal ‘IN’ also shown as the signal ‘Vin’ . . . being fed to a first signal converter stage 105₃, the output of which is fed to signal converter stage 105₂, the output of which is fed to signal converter stage 105₁, etc.” Ex. 1002 ¶ 95 (citing Ex. 1004, Fig. 1, 2:60–3:45). According to Dr. Holberg, “[i]n Figure 2 of Cesura . . . the first signal converter stage 105₃

IPR2020-01561
Patent 7,719,452 B2

is illustrated in detail with its constituent components, whereas the remaining signal converter stages 105_2 , 105_1 , and 105_0 are illustrated collectively by the box ‘STAGES’ 105_{20} .’’ *Id.* (citing Ex. 1004, Fig. 2, 3:46–4:32).

(4) Limitation [1D]

Relying on Dr. Holberg’s testimony, Petitioner argues that Cesura’s DAC 210 responds to a random digital code generated by pseudo random noise generator 205 to generate analog dither signals. Pet. 20 (citing Ex. 1002 ¶¶ 96–97). Petitioner argues that the analog dither signals from DAC 210 are injected into the first signal converter stage 105_3 , as functionally illustrated by being summed with the analog input signal V_{in} at the input node of flash ADC 115 in stage 105_3 . *Id.* (citing Ex. 1002 ¶¶ 96–97). Petitioner additionally argues Cesura discloses that the “resulting analog signal $V_{in}+t$ is applied to the ADC 115, so as to be converted into a corresponding digital signal $V_{in}+eq+t$ (wherein eq is the residue introduced by the quantization error of the ADC 115),” and, thus, signal converter stage 105_3 processes the samples and the analog dither signals into a plurality of digital codes. *Id.* at 21 (citing Ex. 1002 ¶ 98). According to Petitioner, because the stages 105_3 – 105_0 are connected consecutively in a pipeline, the successive stages 105_2 – 105_0 will likewise process the samples and analog dither signals. *Id.* (citing Ex. 1002 ¶ 98).

(5) Limitation [1E]

Petitioner argues that Cesura’s shifter 203, amplifier 220, and adder 235 collectively teach an aligner/corrector as claimed. Pet. 22–24 (citing Ex. 1002 ¶¶ 99–100). Petitioner additionally argues that, to the extent Cesura’s elements 203/220/235 do not expressly provide an “aligner/corrector” function, it would have been obvious to do so, at least in

IPR2020-01561
Patent 7,719,452 B2

part, because “shifter 135 (**orange**) provides an aligner/corrector function by correcting for differing amounts of inter-stage gain at the respective signal converter stages 1053, 1052, 1051, *etc.* (that feeds through to the respective digital codes output from the respective stages). *Id.* at 24 (citing Ex. 1002 ¶ 101).

(6) Limitation [1F]

Petitioner argues that Cesura discloses a decoder comprising amplifier 225, amplifier 230, and LMS logic module 240. Pet. 26 (citing Ex. 1002 ¶ 103). As argued by Petitioner, amplifier 225 receives as its input the signal $V_{in}+eq+t$, applies a gain G thereto, and outputs the amplified signal to amplifier 230, which applies a gain of \hat{e} to the signal. *Id.* (citing Ex. 1002 ¶ 103). Thus, according to Petitioner, amplifiers 225/230 apply a transfer function of $G\hat{e}$ to the $V_{in}-eq+t$ digital signal, including the recited “second portion,” t , that is the random digital code. *Id.* (citing Ex. 1002 ¶ 103). Petitioner further argues that the output of amplifiers 225/230 is applied to adder 235, which “differences” the signals coming from the amplifiers 225/230 with the combined digital code coming collectively from shifter 203 and amplifier 220. *Id.* at 27 (citing Ex. 1002 ¶ 104). According to Petitioner, Cesura’s logic module 240 “calculates the digital correction signal \hat{e} that approximates the digital representation of the analog error e minimizing their difference according to a Least Mean Square Algorithm (LMS)” to ensure that $\hat{e}=e$. *Id.* at 28 (citing Ex. 1002 ¶ 105).

(7) Limitation [1G]

Relying on Dr. Holberg’s testimony, Petitioner argues that Cesura discloses injecting analog dither signals t into the ADC 115 along with the analog input signal V_{in} . Pet. 28 (citing Ex. 1002 ¶ 106). Dr. Holberg testifies that Cesura’s analog dither signals cause at least one, and

IPR2020-01561
Patent 7,719,452 B2

undoubtedly the first and second stages of its pipeline ADC to operate at different operating points, depending on the value of the dither signal at any given moment. Ex. 1002 ¶ 106 (citing Ex. 1004, Fig. 2, 4:8–33); Ex. 2003, 85:9– 86:25. Dr. Holberg further testifies that each operating point in the respective stages represents a signal processing path, and thus, the samples processed by the ADC are processed along a different signal-processing path depending on the value of the dither signal. *Id.* ¶ 106 (citing Ex. 1004, Fig. 2, 4:8–33). Thus, according to Dr. Holberg, Cesura discloses that, as a result of dithering, the samples are processed along different signal-processing paths of said signal converters. *Id.*

(8) Independent Claim 13

Claim 13 differs from claim 1 mainly by eliminating the limitation of “a sampler” as recited in claim [1B], and thus claim [13C] recites, “inject[ing] corresponding analog dither signals into at least a selected one of said signal converters.” Ex. 1001, 17:10–12. The parties acknowledge the main difference “being that in claim [1D] dither can be injected into either the sampler or one of the signal converters.” Pet. 36 (citing Ex. 1002 ¶¶ 120–121); *see also* PO Resp. 41 (Patent Owner confirming that “[c]laim 13 has different phrasing, stating that the dither is injected into one of the converters.”).

b) Patent Owner’s Arguments

Patent Owner’s arguments are premised mainly on their incorrect claim construction that claims 1 and 13 require “dither injected into **one** of the ADC’s sampler or pipelined stages would propagate through **all** of the downstream stages of the pipelined converter system.” PO Resp. 1–2. Patent Owner argues that “[n]either the Petition nor the art itself contains any discussion of whether the cited art’s purported ‘dither signals’ cause the

IPR2020-01561
Patent 7,719,452 B2

input samples to be processed along different signal-processing paths in *all* stages of a pipelined converter system.” *Id.* at 2.

As discussed above in our claim construction analysis, Patent Owner applies a name for the problem alleged to be solved by the ’452 patent, that is—“dither exhaustion.” *Id.* at 10 (citing Ex. 2002 ¶ 30). Patent Owner argues specifically that “[t]he ’452 inventors demonstrate the problem addressed by the patent—dither exhaustion—in Figures 7A and B of the patent.” *Id.* Patent Owner provides the annotated Figure 10 from the ’452 patent, reproduced below, to illustrate “dither exhaustion.”

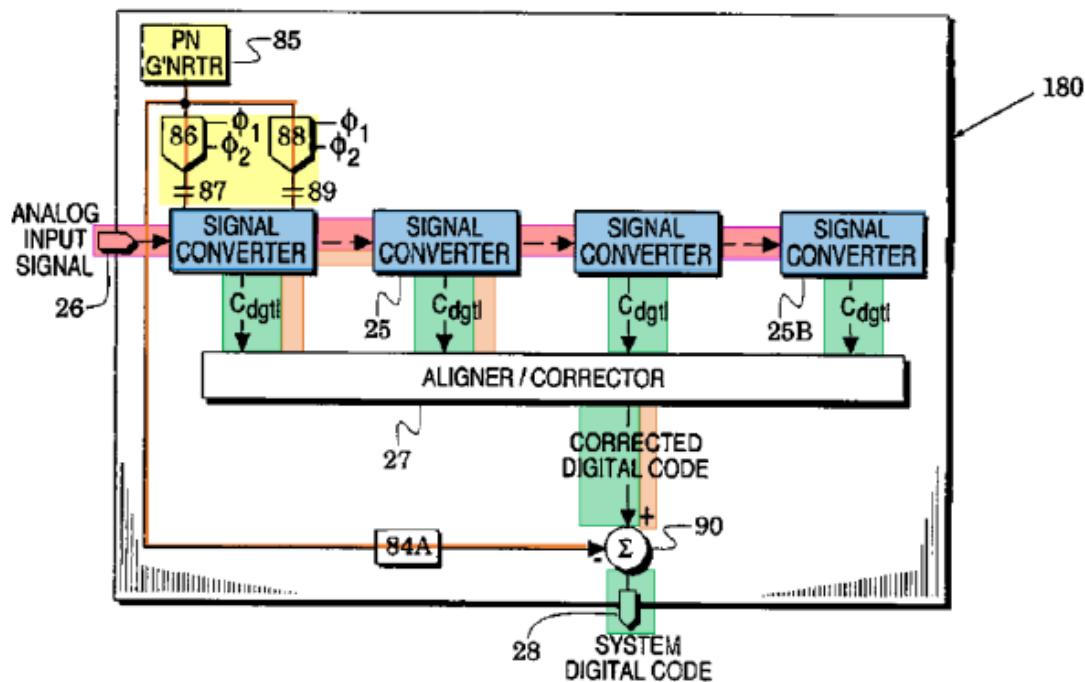


Figure 10 of the ’452 patent, as annotated by Patent Owner, illustrates a pipelined converter system with PN generator 85 adding a dither signal into the first signal converter via DACs 86, 88. *Id.* at 12. Patent Owner argues that “in this example, the dither is exhausted by the third converter stage (and for all

IPR2020-01561
Patent 7,719,452 B2

subsequent converter stages), and from the perspective of these stages, it is as though dither was never injected into any stage of the pipeline.”⁶ *Id.* (citing Ex. 2002 ¶ 32).

Similar to its arguments with respect to claim construction, Patent Owner argues that Figure 7A, reproduced below as annotated by Patent Owner, illustrates the problem of dither exhaustion. *Id.* at 16.

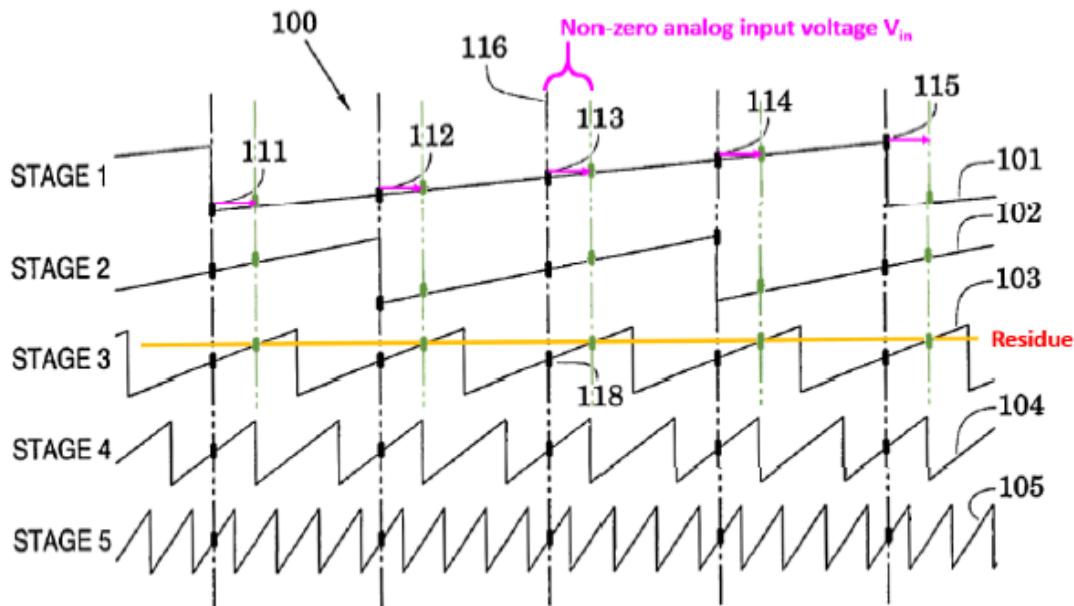


FIG. 7A

Figure 7A, as annotated by Patent Owner, illustrates one embodiment of the converter system in Figure 6 where stages 1 and 2 process the respective combined signal (101–102) at different operating points. *Id.* Patent Owner contends that Figure 7A “shows that the residue value in converter stage 3 is the same regardless of the dither level injected into stage 1, which indicates that the dither has been exhausted.” Ex. 2002 ¶ 43.

⁶ Patent Owner’s brief includes color-coded wording coordinated with the colors in the drawings. We do not reproduce the color-coded wording in this Decision.

IPR2020-01561
Patent 7,719,452 B2

Patent Owner argues that the problem of dither exhaustion is solved by the claimed invention and is illustrated by annotated Figure 7B reproduced below.

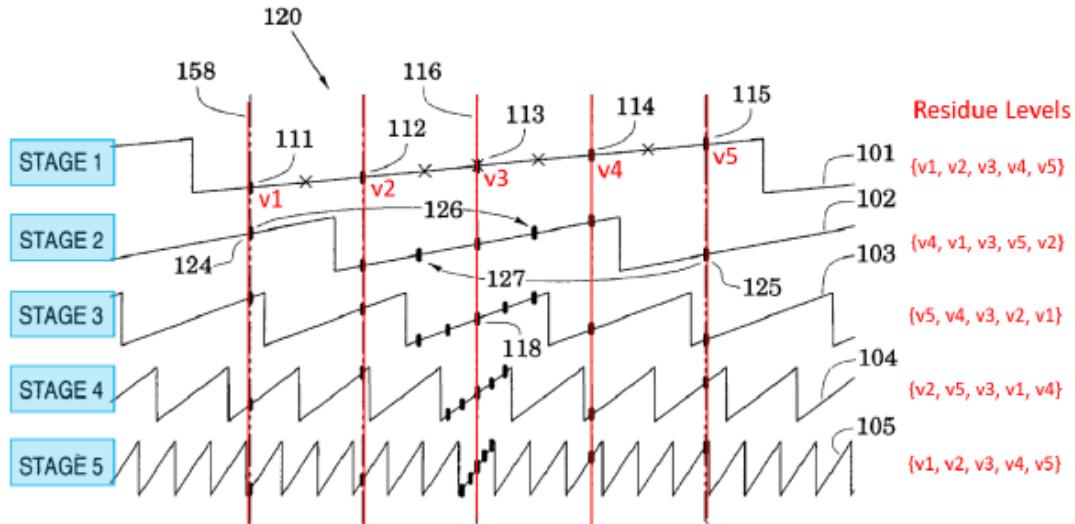


FIG. 7B

Figure 7B, above, illustrates, compared to Figure 7A, a preferred result where each stage 1–5 processes the combined signal (101–105) at different operating points. PO Resp. 17. Patent Owner argues that “Figure 7B depicts the operation of the claimed pipelined converter in which *all* of the pipelined stages receive the randomizing, error-averaging benefits of dither.” *Id.* at 16.

In addition to the “dither exhaustion” and intertwined claim construction arguments noted here, Patent Owner makes additional arguments with respect to Cesura as it pertains to independent claims 1 and 13 which we address in our analysis below.

c) Analysis

With respect to claim limitations [1A]–[1C] and [1E], we have reviewed Petitioner’s arguments and the underlying evidence cited in support and are persuaded that Petitioner sufficiently establishes that Cesura

IPR2020-01561
Patent 7,719,452 B2

discloses these limitations. Patent Owner's arguments mainly pertain to limitations [1D], [1F], and [1G], which we address below.

It is very helpful in our analysis to understand *why*, according to the '452 patent, a better or more preferred result is obtained in Figure 7B.

The '452 patent explains that for Figure 7A

[i]t is further assumed that the PN generator **81**, DAC **82** and at least one capacitor **83** are configured to dither this operating point over five operating points **111**, **112**, **113**, **114** and **115** (in FIG. 7A, each operating point is indicated by an oblong marker) wherein operating points **111** and **115** coincide with the ends of the converter subrange.

Ex. 1001, 7:23–29. Thus, according to the '452 patent, the five dithered operating points 111–115 shown in Figure 7A, “coincide with the ends of the converter subrange,” i.e., at the lowest and highest sawtooth points (111, 115), in stage 1, and therefore span the output-signal window. *Id.*

Configuring PN generator 81, DAC 82 and capacitor 83, in this way results, apparently, in “the dither fail[ing] to alter the signal processing path through these latter stages.” *Id.* at 7:56–57.

To resolve this problem, the '452 patent describes that in Figure 7B “the five dithered operating points are now arranged so that they span substantially 4/5 of the output signal window, i.e., the span between operating points 111 and 115 is substantially 4/5 of the output-signal window.” *Id.* at 7:64–66. Observing Figure 7B, the operating points in stage 1 are now configured to *not* coincide with the lowest and highest sawtooth, and therefore span the 4/5 of the output signal window. The '452 patent sums this up by explaining that it is beneficial to select

a predetermined dither range which sufficiently differs from the output-signal window of the selected stage so that, in each of

IPR2020-01561
Patent 7,719,452 B2

succeeding stages, the respective dither range covers a substantial portion of the respective output-signal window

Ex. 1001, 8:55–59.

Considering these examples and the written description and figures of the '452 patent, we agree with Patent Owner's statement that “[a]s the inventors observed, the use of such specific configurations of dither signals could ensure that an injected dither signal would propagate to each converter stage in the pipeline.” PO Resp. 20 (citing Ex. 1001, 14:39–52). However, notably, neither of the independent claims 1 or 13 include any limitations relating to a dither range covering any portion of the output-signal window.

In any event, as discussed above, the proper claim construction for limitation 1[G] is not limited to processing samples along “*all* said signal converters” in the claimed analog-to-digital converter system. Therefore, we disagree with Patent Owner's overall conclusion that “[b]oth independent claims capture this invention.” *Id.* at 21.

Turning to Cesura, Patent Owner argues that “Cesura contains no mention of a digital-to-analog converter (DAC) configured to inject dither signals in a manner that ensures *all* pipeline stages of the ADC benefit from the randomizing effect of the dither signal (i.e., that the dither does not exhaust after some stages of processing).” PO Resp. 36–37. The proper claim construction, however, does not require “*all* pipeline stages of the ADC benefit from the randomizing effect of the dither signal,” as Patent Owner argues. *Id.* at 37.

Besides reiterating that Patent Owner's claim construction is erroneous, Petitioner replies that Dr. Holberg's testimony unmistakably explains, both in his original declaration and subsequently under cross-examination, that Cesura discloses successive stages 105₂–105₀ processing

IPR2020-01561
Patent 7,719,452 B2

the input signal samples and dither injected into Cesura's first stage 105₃. Dr. Holberg's testifies in his original declaration that

signal converter stage 105₃ "process[es] said analog samples and said analog dither signals into a plurality of digital codes" as recited by this claim element. Because the stages 105₃ - 105₀ are connected consecutively in a pipeline (the output of one stage feeding the next stage), the successive stages 105₂ - 105₀ will likewise process the samples and analog dither signals into respective digital codes.

Ex. 1002 ¶ 98. During Dr. Holberg's deposition, Patent Owner's counsel asked whether Cesura's Figure 2 showed processing of the combined input signal residue and dither signal by the successive stages 105₂ - 105₀:

Q: So in Figure 2, Stages 105/20 represent Stages 105/2, 105/1, and 105/0, shown in the prior art Figure 1, correct?

A: Correct.

Q: And so Figure 2 does not represent an embodiment where the correction circuitry is applied to Stages 105/2, 105/1, or 105/0, correct?

A: [T]his figure doesn't.

Ex. 2003, 83:1–9. Although agreeing that Cesura's Figure 2 did not show processing by the successive stages 105₂ - 105₀, Dr. Holberg explained with more clarity why Cesura, as a whole, does disclose that the successive stages 105₂ - 105₀, in addition to the initial stage 105₃, also process the combined input sample $V_{in} + t$ (where t is the added dither signal):

Q. Did you do any analysis of whether Stages 105/2, 105/1, and 105/0 process their analog input signals down different paths based on test signal t ?

...

A. Well, claim 1G of '452 says, "samples thus processed along different signal-processing paths of signal

IPR2020-01561
Patent 7,719,452 B2

converters to thereby enhance linearity of said system.” So I said, “Cesura discloses injecting an analog to the signal t into the ADC 115 along with the analog input signal. Cesura’s analog dither signals will cause at least one stage of the pipeline to operate at different points depending on the value of the dither signal in any given moment . . . [“] So, I mean, I said here that at least one of the stages. But, you know, sitting here today, you know, looking at it, you know, in a different light, based upon your question, it appears that Cesura, as I read in the passage, you know, he says that you can apply the tests over one or more stages. And the output of the first stage has the -- has the test signal embedded in it, which is something I really didn’t think about before. But that signal is patched onto the subsequent stages as well.

Id. at 85:9– 86:25.

In this line of questioning by Patent Owner’s counsel, Dr. Holberg was consistent, explaining that because the output of the first stage 105_3 included dither signal t output to second stage 105_2 , then the dither signal would indeed be applied to multiple stages:

Q. So I’m talking about an embodiment in which test signal t is inserted only into Stage 105/3. Okay? In that embodiment, would Stage 105/1 process a signal down different paths based on test signal t ?

...

A: Well, given -- it might, given that the output V_{out} is G plus e times the quantity negative eq minus t . So V_{out} has t in it, and that’s going to the subsequent stages.

Id. at 88:8–18. Dr. Holberg was clear in his deposition that although Figure 2, which is a circuit diagram, does not show specific processing being carried out by subsequent stages, a person of ordinary skill in the art would understand that this is undoubtedly occurring:

IPR2020-01561
Patent 7,719,452 B2

Q. And today you have no idea whether the output of Stage 105/2 includes a component based on t , do you?

A. That's not described in this figure. But a POSITA looking at it would -- and reading that paragraph that I just read that the algorithm could apply to one or more stages, that maybe it does.

Id. at 89:4–11.

Patent Owner's declarant, Dr. Moon, testifies that "Cesura . . . says nothing about processing an injected random signal in *any* succeeding stage of an ADC, much less a DAC configured to inject a dither signal that is processed by *all* the succeeding stages." Ex. 2002 ¶ 64. We appreciate that Cesura discusses mainly that dither signal t is added via PRN generator 205 and DAC 210 to initial stage 105₃, however, we find Dr. Holberg's testimony on this point more persuasive, specifically that in Cesura "the output voltage of one stage is the input voltage of the next stage. We can't dispute that. And [] that output voltage has a t in it." Ex. 2003, 90:22–24. Indeed, we have no persuasive testimony from Dr. Moon that the combined input and test dither signal *would not* be processed by subsequent stages. For example, Dr. Moon testifies that "Cesura does not teach or suggest that its test signals propagate to downstream stages 105₁ and 105₀, and provides no reason to believe that they would." Ex. 2002 ¶ 67. Dr. Moon essentially repeats Patent Owner's "dither exhaustion" argument, yet conspicuously does not include stage 105₂, which immediately follows the initial stage 105₃ in Cesura's pipelined converter. Ex. 1004, Fig. 1. This is, in effect, consistent with Dr. Holberg's testimony that the output of initial stage 105₃ includes the test signal and thus a person of ordinary skill in the art would have understood that it is also the input signal to be processed by subsequent stage 105₂.

We are persuaded by the arguments and evidence of record that a person of ordinary skill in the art would have understood that Cesura's test signal t is applied to multiple stages of the signal converter system.

Besides the issue of claim construction and the interpretation of Cesura's disclosure, Patent Owner makes several other arguments with respect to Cesura. First, that "Cesura does not teach or suggest processing dither through all the signal converters in an ADC system." PO Resp. 40–44. Second, Patent Owner argue that "Cesura does not teach or suggest 'said samples thus processed along different signal-processing paths of said signal converters'" as recited in independent claim 1G and 13F. *Id.* at 44–46. Third, Patent Owner argues that "Cesura does not teach or suggest 'an aligner/corrector . . . to process said plurality of digital codes into a combined digital code'" as recited in claims 1E and 13D. *Id.* at 46–48. Fourth, Patent Owner argues that "Cesura does not teach or suggest 'a decoder having a transfer function configured to convert said random digital code to said second portion for differencing with said combined digital code'" as recited in claim limitations 1F and 13E. *Id.* at 48–57. We address these arguments in turn.

(1) Whether Cesura teaches processing dither through all the signal converters in an ADC system

The issue of whether or not Cesura teaches processing dither through all the signal converters in an ADC system is based on Patent Owner's erroneous claim construction. *Id.* at 41. As discussed above, the claim language does not require that dither is processed through "all said signal converters," and we are persuaded that a person of ordinary skill in the art would have understood that Cesura teaches processing combined input and dither samples through multiple signal converters in an ADC system.

IPR2020-01561
Patent 7,719,452 B2

(2) *Whether Cesura teaches “said samples thus processed along different signal-processing paths of said signal converters”*

This argument is also based on Patent Owner’s erroneous claim construction, that independent claims 1 and 13 “be construed to require that the input samples be processed along different signal-processing paths in **each** of the **multiple** stages of the converter system.” *Id.* at 44. For the same reasons as discussed above, we do not find this argument persuasive.

(3) *Whether Cesura teaches “an aligner/corrector . . . to process said plurality of digital codes into a combined digital code”*

Patent Owner argues that Petitioner has failed to show that Cesura’s elements shifter 203, multiplier 220, and adder 235, correspond to an aligner/corrector as recited in independent claims 1 and 13. *Id.* at 46. The reason Patent Owner contends is that “in Figure 2 of Cesura adder 235 combines **three** inputs, not **two**, to create an output signal OUT that is represented by the expression ‘ $V_{in}(1 + \hat{e})G + (eq + t)G(\hat{e} - e)$ ’. **Nowhere** does Cesura describe forming the combined digital code alleged by the Petition.” *Id.* at 46–47.

The Petition explains that Cesura’s shifter 203 is coupled to multiple converter stages 105₂₀, and processes the digital code which has two terms, the first term corresponding to the input signal samples, and the second term corresponding to the analog dither signals. Pet. 22 (citing Ex.1002 ¶ 99). According to Petitioner, amplifier 220 processes a digital code from the first signal converter 105₃, this code also including a first term corresponding to the input samples, and a second term corresponding to the analog dither signals. *Id.* at 23. Dr. Holberg testifies that

IPR2020-01561
Patent 7,719,452 B2

Adder 235 combines the digital code from amplifier 220 with digital codes from shifter 203 together to form a combined digital code, namely $[(\text{-eq-t})G(l+e)] + [(\text{Vin} + \text{eq} + t)G] = [(\text{GVin} - G(e)(\text{eq})) - G(e)(t)]$, that includes a first portion, $(\text{GVin} - G(e)(\text{eq}))$, corresponding to said samples and a second portion, $- G(e)(t)$, corresponding to said analog dither signals.

Ex. 1002 ¶ 100 (citing Ex. 1004, 3:46–4:32, Fig. 2).

The '452 patent describes that “aligner/corrector 27” receives the digital codes from all the signal converter stages and “only after the aligner/corrector 27 has received the digital codes C_{dgl} from all of the signal converters 25, does it provide a system digital code at an output port 28 that corresponds to the original sample.” Ex. 1001, 3:6–10. Similarly, we understand from a plain reading of claim 1 that the claimed aligner/corrector “process[es] said plurality of digital codes into a combined digital code that includes a first portion that corresponds to said samples and a second portion that corresponds to said analog dither signals.” *Id.* at 16:8–11. The claim language does not recite any limitations as to specifically *how* the process of a combined digital code is carried out, what order the signals are added to provide the output digital code, or that the output digital code is limited to only two inputs. Therefore, we find that a person of ordinary skill in the art would have understood that Cesura teaches an aligner/corrector as claimed, and Patent Owner’s explanation, evidence and arguments are unpersuasive.

(4) *Whether Cesura teaches “a decoder having a transfer function configured to convert said random digital code to said second portion”*

Patent Owner explains that “a decoder converts the initial random digital code used to generate the injected analog dither signal into a ‘second portion,’ which is then subtracted from the combined digital code to derive the final ‘system digital code’ corresponding to the analog sample.” PO

IPR2020-01561
Patent 7,719,452 B2

Resp. 48. But, According to Patent Owner, “nothing in Cesura corresponds to a decoder that applies a transfer function to ‘t’ to generate the claimed ‘second portion’ or differences that ‘second portion’ from a ‘combined digital code.’” *Id.* at 50.

In the Petition, Petitioner explained that in Cesura’s Figure 2 amplifiers 225 and 230 together apply a transfer function $G\hat{e}$ to input $V_{in}+eq+t$, including the dither signal t , resulting in $(V_{in}+eq+t)G\hat{e}$. Pet. 26 (citing Ex. 1002 ¶ 103). Dr. Holberg testifies persuasively that

Figure 2 also illustrates that the output of amplifiers 225/230 is applied to adder 235, which “differences” the signals coming from the amplifiers 225/230 with the combined digital code coming, collectively, from shifter 203 and amplifier 220 . . . it is self-evident that the summing of the “ t ” component (from the amplifiers 225/230) and the “ $-t$ ” component (from the shifter 203) is equivalent to the difference in the magnitudes of the respective “ t ” components.

Ex. 1002 ¶ 104.

Patent Owner argues that different from the claimed invention “Cesura requires that the ADC output (the OUT signal) **contain** a component corresponding to the test signal so that LMS module 240 may correlate the test signal with the ADC output to drive the estimation of ‘ \hat{e} ’” PO Resp. 49. In other words, Patent Owner argues that test signal t has not been removed from the Cesura’s output signal, because to do so would eliminate feedback to amplifier 230 as shown in Cesura’s Figure 2.

Petitioner responds in two ways, first, pointing out that contrary to Patent Owner’s assertion Cesura explicitly states that

[i]n the ideal condition wherein $e=e$, the digital output signal OUT is then equal to $V_{in}(1+e)G$. In this way, the additive term (including the digital test signal t) due to the analog error e of the amplifier 130 providing the inter-stage gain *is deleted*; therefore,

IPR2020-01561
Patent 7,719,452 B2

the harmonic distortion caused by the imprecision of the inter-stage gain is eliminated, or at least substantially reduced.

Reply 11 (citing Ex. 1004, 4:57–63) (emphasis added). Second, to the extent that the ideal condition does not exist and the test signal is not deleted, Petitioner points out persuasively that the claims do not recite that the dither must be deleted or “removed.” *See id.* (Petitioner arguing that the independent claims “only recite ‘differencing’ the second portion (which corresponds to the dither signal) with the combined digital code.”). We find Dr. Holberg’s testimony on this point persuasive. Dr. Holberg testifies that

[i]n indeed, Cesura’s logic module 240 “calculates the digital correction signal \hat{e} that approximates the digital representation of the analog error e minimizing their difference according to a Least Mean Square Algorithm (LMS)” to ensure that $\hat{e}=e$. []. Stated another way, the portion of the digital output code corresponding to the dither signal “ t ” that was injected into the pipeline is effectively removed by the transfer function of amplifiers 225/230 and LMS logic module 240. Hence, Cesura discloses this claim limitation.

Ex. 1002 ¶ 105.

Patent Owner argues also that Petitioner has taken inconsistent positions as to what exactly is the claimed “second portion,” i.e., whether the “second portion” is $G(e)(t)$ or $-G(e)(t)$. PO Resp. 51 (citing Pet. 23). Patent Owner argues that “the sign of ‘ $-G(e)(t)$ ’ is negative, not positive. As such, ‘ $-G(e)(t)$ ’ cannot comprise a portion of anything, because the ‘-’ sign indicates this [] term is *missing* from that output.” *Id.*

Petitioner responds that such an assertion is unsupported by Cesura’s disclosure and inconsistent with the electrical convention and the understanding of a person of ordinary skill in the art. Reply 11–12. Petitioner contends that a person of ordinary skill in the art “would readily understand that a ‘-’ sign indicates a signal having a magnitude that can be

IPR2020-01561
Patent 7,719,452 B2

summed and/or differenced with other signals.” *Id.* at 12 (citing Ex. 1002 ¶ 104). Petitioner points out that Cesura’s Figure 2 explicitly discloses the output of shifter 203 includes a signal having an -eq-t component. *Id.* (citing Ex. 1004, Fig. 2). Dr. Holberg testifies

that the “eq” component and the “t” component of the digital signal from shifter 203 are both of opposite polarity (*i.e.*, “-eq” and “-t”) relative to the “eq” and “t” components of the signals coming from the amplifiers 225/230 (and also from amplifier 220) - *and hence adder 235 results in the difference of the respective components when they are added together.*

Ex. 1002 ¶ 104 (emphasis added). We find more persuasive Dr. Holberg’s testimony that the “-” sign is an indication of polarity, not that it is “missing” as Dr. Moon testifies. *See* Ex. 2002 ¶ 72 (Dr. Moon stating that “‘-G(e)(t)’ cannot comprise a portion of anything, because the ‘-’ sign indicates this is term is *missing* from that output.”). The specification clearly describes voltage signals as comprising positive and negative components. *See, e.g.*, Ex. 1004, 4:18–22 (Cesura explaining that test signal t could be “for example, -10 mV for the logic value 0 and +10 mV for the logic value 1”). Our review of Cesura is more consistent with Petitioner and Dr. Holberg’s assertions that Cesura considers the “-” sign as a sign of polarity.

Claim limitation 1[F] requires that the decoder convert the “random digital code” (that generates the dither signal in limitation 1[C]), into “said second portion” of the combined digital code that corresponds to the analog dither signals. Considering Cesura’s Figure 2, Petitioner explains that this limitation is encompassed by Cesura’s adder 235 receiving signal $(V_{in}+eq+t)G_e$ from amplifiers 225/230, and adding this to the signal $(-eq-t)G(l+e)$ from shifter 203, to generate the

IPR2020-01561
Patent 7,719,452 B2

combined digital code output of the ADC that is “ $V_{in}(1+\hat{e})G+(eq+t)G(\hat{e}-e)$ ”. Reply 12 (citing Ex. 1002 ¶ 4). Overall, we find persuasive Petitioner’s position with respect to the decoder’s “differencing” function as recited in limitation [1F], that “Cesura discloses adding signals having opposite polarity ($A+(-B)$), which is equivalent to the claimed element of “differencing” two signals ($A-B$), as Holberg demonstrated.” Reply 13 (citing Ex. 1002 ¶¶104–105).

One last thing on this particular argument by Patent Owner. To the extent that Patent Owner is arguing that Petitioner is asserting two different signals from Cesura, i.e., “ $-G(e)(t)$ ”, and “ $+G(e)(t)$ ” for the “second portion” this argument misinterprets Patent Owner’s own claim language. On its face, claim limitation [1E] clearly recites that the “second portion” corresponds to the claimed analog dither signals, not any particular value or signal. *See* Ex. 1001, 16:10–11 (Claim 1 reciting “a second portion that corresponds to said analog dither signals”). Indeed, if this were not the case, it is unclear how the “combined digital code” in limitation [1E] could be “differenced” with itself, in order to determine a final “system digital code.” We do not find Patent Owner’s arguments here compelling.

Having considered the entire record now before us, including the arguments and evidence presented by both parties, we are persuaded by Petitioner’s arguments and evidence that claims 1 and 13 would have been obvious over Cesura.

3. *Claims 2 and 14*

Claims 2 and 14 require “a differencer to difference said second portion and said combined digital code to provide said system digital code.” Patent Owner argues that Cesura discloses only adder 235 “and does not

IPR2020-01561
Patent 7,719,452 B2

calculate a difference between any of its input values.” Patent Owner contends that no matter the values processed by adder 235, the “adder 235 still performs only *additions* on those components and does not perform any differencing as required by the claim.” PO Resp. 57 (citing Ex. 2002 ¶ 79).

Petitioner responds, arguing that the ’452 patent uses the terms “summer” and “differencer” interchangeably. *See* Reply 15 (citing Ex. 1001, 7:46–61) (the ’452 patent describing element 90 in Figure 6 as a “summer”); *see also id.* at 13:36–41 (the ’452 patent describing element 90 in Figure 6 as a “differencer”). Petitioner contends that the difference between a “differencer,” a “summer,” and an “adder,” “is in fact a distinction without a difference” and points out that regardless of the terminology used, both the ’452 patent at Figure 6 and Cesura show a similar conventional schematic symbol to represent this element. *Id.* at 15–16. Petitioner argues that no matter what you call the summing element, “a POSITA would understand that Cesura’s adding of two signals (having opposite polarity) is functionally the same as finding a difference of two signals of the same polarity.”

We acknowledge that addition is a different mathematical operation from subtraction, and “differencing.” However, Petitioner’s position is compelling that a person of ordinary skill in the art would understand that an “adder” as described by Cesura, and a “differencer” as recited in the claims of the ’452 patent, are functionally and structurally equivalent. The ’452 patent clearly conflates the element of summer 90, and differencer 90. *Compare* Ex. 1001, 7:46–61, *with id.* at 13:36–41. With respect to Cesura calling a similar element an “adder 235,” Dr. Holberg explains persuasively that “[b]ecause the “t” components of these signals have opposite polarity

IPR2020-01561
Patent 7,719,452 B2

(“t” and “-t”) adding the signals results in the difference in the magnitude of the respective components. Hence, adder 235 is a “differencer” as claimed.” Ex. 1002 ¶ 110. Although Cesura does not call “adder 235” a “differencer,” we credit Dr. Holberg’s testimony on this point. Moreover, Patent Owner does not explain persuasively that there is any tangible structural or functional difference between these elements. Accordingly, we are persuaded that Petitioner has shown by a preponderance of the evidence that a person of ordinary skill in the art would understand Cesura’s adder as a summer element that is at least equivalent functionally to the claimed “differencer.” It is well-settled that “[a] reference need not teach a limitation *in haec verba.*” *In re Bode*, 550 F.2d 656, 660 (CCPA 1977).

Having considered the entire record now before us, including the arguments and evidence presented by both parties, we are persuaded by Petitioner’s arguments and evidence that claims 2 and 14 would have been obvious over Cesura.

4. *Claims 8, 9, 15, and 16*

Petitioner argues for claims 8 and 15, similar to limitation [1D], that “Cesura’s signal converters (stages 105₃-105₁) are configured to provide analog output signals to succeeding signal converters.” Pet. 32 (citing Ex. 1002 ¶ 113. Petitioner explains that because Cesura’s pipelined converters 105₂-105₁ are configured to receive an input signal from a preceding converter “each converter stage (except the last one) provides a residue signal with an amplitude limited to an output-signal window (*i.e.*, the input range of the next stage). *Id.* at 33–34 (citing Ex. 1002 ¶ 114).

Petitioner argues for claims 9 and 16, that Cesura teaches a dither range “lower than a half LSB of the ADC 115.” *Id.* at 35 (citing Ex. 1002 ¶ 116). Petitioner contends that

IPR2020-01561
Patent 7,719,452 B2

Cesura further discloses that stage 105₃, which contains the ADC 115 is a four bit stage. [] Since +/-10 mV is a half LSB for this ADC, then one LSB is +/- 20 mV. Hence, the stage must be capable of an output window of at least +/- 320 mV, meaning that the predetermined dither window of +/-10 mV is less than this output-signal window.

Id.

Patent Owner argues that claims 8, 9, 15, and 16 depend either directly or indirectly from independent claims 1 and 13, and are not obvious for the same reasons as the independent claims. PO Resp. 57.

Having considered the entire record now before us, including the arguments and evidence presented by both parties, we adopt and incorporate Petitioner's showing as to claims 8, 9, 15, and 16, as set forth in the Petition and summarized above, as our own. *See* Pet. 32–35, 38. Accordingly, we are persuaded by Petitioner's arguments and evidence that claims 8, 9, 15, and 16 would have been obvious over Cesura.

C. Obviousness over Cesura, Lewis, and Bjornsen

Petitioner argues that claims 12 and 19–20 would have been obvious over the combination of Cesura, Lewis, and Bjornsen. Pet. 38–52. Having reviewed the information provided by Petitioner, including the relevant portions of the supporting Holberg Declaration, we are persuaded, on the current record, that Petitioner has demonstrated by a preponderance of the evidence that the challenged claims would have been unpatentable over Cesura, Lewis, and Bjornsen.

1. Lewis (Ex. 1006)

Lewis describes a pipelined, 5-Msample/s, 9-bit analog-to-digital (A/D) converter designed and fabricated in CMOS technology. Ex. 1006,

IPR2020-01561
Patent 7,719,452 B2

954.⁷ An example of the pipelined A/D converter is illustrated in Figure 1, reproduced below.

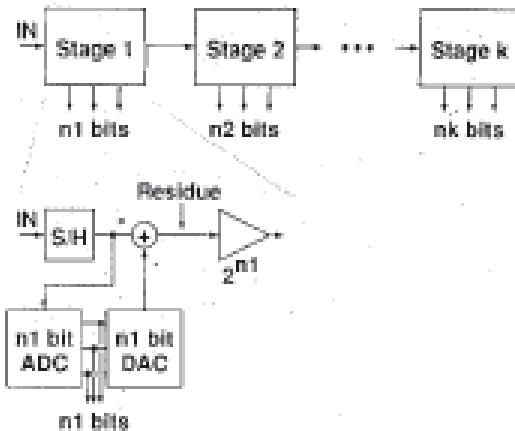


Fig. 1. Block diagram of a general pipelined A/D converter.

Figure 1, above, illustrates a block diagram of a general pipelined A/D converter with k stages. *Id.* Each stage contains an S/H circuit, a low-resolution A/D subconverter, a low-resolution D/A converter, and a differencing fixed-gain amplifier. *Id.* Each stage then does a low-resolution A/D conversion on the held input, and the code just produced is converted back into an analog signal by a D/A converter. *Id.* Finally, the D/A converter output is subtracted from the held input, producing a residue that is amplified and sent to the next stage. *Id.*

Figure 4, reproduced below, illustrates an example of a two-stage pipelined A/D converter.

⁷ We refer here, to the actual IEEE Journal page numbers.

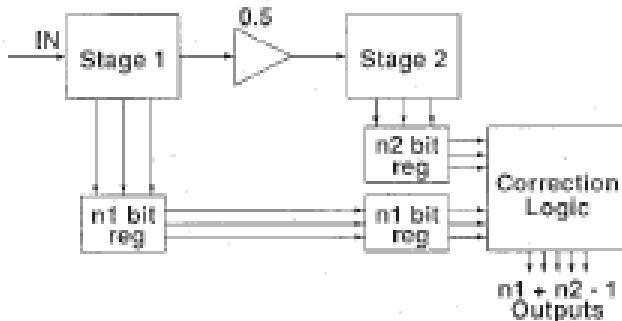


Fig. 4. Block diagram of a two-stage pipelined A/D converter with digital correction.

Figure 4, above, illustrates a block diagram of a two-stage pipelined A/D converter with digital correction. *Id.* at 956. The new elements in this diagram are the pipelined latches, the digital correction logic circuit, and the amplifier with a gain of 0.5. *Id.*

Lewis describes that 1 bit from the second stage is saved to digitally correct the outputs from the first stage; the other $n2 - 1$ bits from the second stage are added to the overall resolution. *Id.* After the pipelined latches align the outputs in time so that they correspond to one input, the digital correction block detects overrange in the outputs of the second stage and changes the output of the first stage by 1 LSB at $n1$ -bit level if overrange occurs. *Id.*

2. Bjornsen (Ex. 1007)

Bjornsen describes an analog-to-digital converter (ADC) circuit that converts an analog input signal into a digital output signal, where the ADC circuit includes a noise shaping first stage cascaded with a pipelined second stage. Ex. 1007, 2:53–56. The first stage includes a sample-and-hold circuit and a first order modulator, where the first order modulator includes a noise shaping filter, a FLASH ADC and a feedback digital-to-analog converter (DAC). *Id.* at 2:56–59. A digital dither generator is used to provide a dither signal to the ADC circuit. *Id.* at 2:59–60.

IPR2020-01561
Patent 7,719,452 B2

Figure 6, reproduced below, illustrates an example circuit diagram of a multiplying and integrating DAC (MDAC) used in a first order modulator.

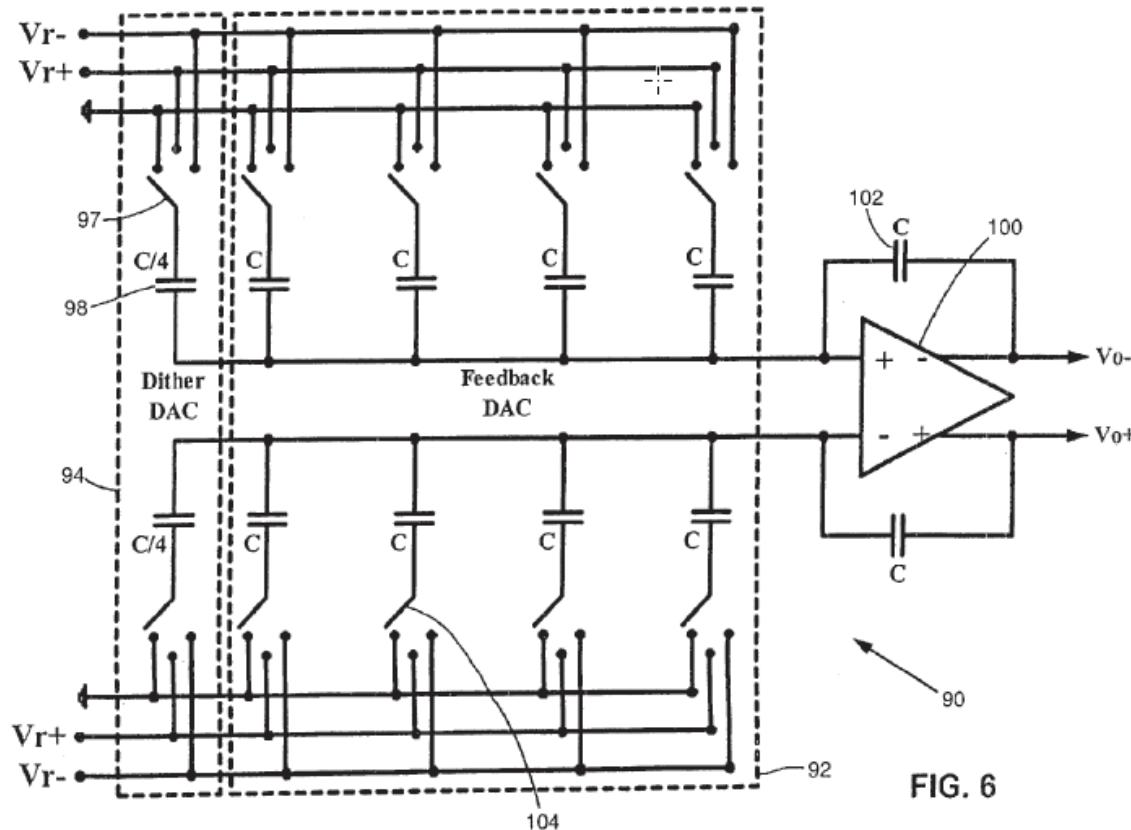


Figure 6, above, shows a MDAC 90 be in used in a feedback phase of a modulator 50. *Id.* at 6:57–59, 7:3–4. The MDAC 90 consists of a regular feedback DAC 92 and a dither DAC 94. *Id.* at 6:59–60. The regular feedback DAC 92 includes unit capacitors 96, each having the size of C, and the dither DAC 94 include dither capacitors 98, each having a size of C/4. *Id.* at 6:60–63. Dither capacitors 98 provide a dither signal to dither DAC 94. *Id.* at 7:23–26.

3. Dependent claims 12, 19, and 20

Claim 12 depends directly from claim 8 and recites

wherein said selected signal converter includes at least first and second dither capacitors and said digital-to-analog converter is configured to switchably couple different voltages to said first

IPR2020-01561
Patent 7,719,452 B2

dither capacitor to thereby contribute to said analog dither signals and switchably couple different voltages to said second dither capacitor to thereby contribute to a respective one of said plurality of digital codes.

Ex. 1001, 16:63–17:3. Claims 19 and 20 each depend directly from claim 15 and recite similar limitations. *Id.* at 18:20–29. Petitioner argues Cesura discloses DAC 210 that injects analog dither signals “t” into the first stage 105₃ of the pipeline. Pet. 45 (citing Ex. 1002 ¶¶ 146, 153, 156). While Petitioner concedes, “Cesura provides no details regarding the specific circuitry in order to realize these functions,” Petitioner further argues “Lewis and Bjornsen provide the type of circuit details that Cesura does not.” *Id.* at 46 (citing Ex. 1002 ¶¶ 147, 154, 157). Petitioner further contends that Dr. Holberg identifies several different reasons why a person of ordinary skill in the art would have been motivated to combine Cesura, Lewis, and Bjornsen. *Id.* at 39–43 (citing Ex. 1002 ¶¶ 132–144).

Dr. Holberg testifies that as shown by Cesura, ADCs typically employ a sample and hold circuit, a sub-ADC circuit, sub-DAC circuit, and an adder. Ex. 1002 ¶ 129. According to Dr. Holberg these are well-known circuits and components of an ADC to those of ordinary skill in the art, and “[a] POSITA would require no details regarding the specific elements (capacitors, operational amplifiers, and the like) to understand the respective elements’ purpose and function.” *Id.* Dr. Holberg explains however, that Lewis and Bjornsen “do provide the circuit details that a POSITA would naturally look to in order to implement the functionality disclosed by Cesura.” *Id.* Dr. Holberg testifies further that the specifics of these type of ADC components were well-known and that

Lewis discloses the details regarding, *e.g.*, a basic switched capacitor implementation for the components. Ex. 1006, pp. 954–

959. Similarly, Bjornsen also discloses an ADC system employing common switched capacitor techniques for implementing the circuit components, and further discloses using a switched capacitor circuit for, *e.g.*, injecting dither signals into the system.

Id. ¶ 132 (citing Ex. 1007, Figs. 2, 5, 6, 9). Based on the level of ordinary skill in the art, as well as the asserted well-known technology and circuit structure of such components, Dr. Holberg testifies that “[t]hese types of circuits are basic building blocks for analog circuits and are readily substituted one for another. . . the results of such substitution would have been predictable to a POSITA.” *Id.* ¶ 134.

Patent Owner does not expressly dispute the combination of Cesura, Lewis, and Bjornsen, but argues that neither Lewis nor Bjornsen teach or discloses “configuring a DAC to ensure that the injected dither propagates to all stages of a pipelined converter.” PO Resp. 58 (citing Ex. 2002 ¶ 81).

Because, as discussed above, we do not agree with Patent Owner’s claim interpretation, and now having considered the entire record now before us, including the arguments and evidence presented by both parties, we adopt and incorporate Petitioner’s showing as to claims 12, 19, and 20, as set forth in the Petition and summarized above, as our own. *See* Pet. 38–52. Based on the entire record, we are persuaded that Petitioner has shown by a preponderance of the evidence that claims 12, 19, and 20 would have been obvious over Cesura, Lewis, and Bjornsen.

D. Obviousness over Fu and Lewis

Petitioner argues that claims 1–4, 8, 9, and 13–16 of the ’452 patent would have been obvious over Fu and Lewis. Having reviewed the information provided by Petitioner, including the relevant portions of the supporting Holberg Declaration, we are persuaded, on the current record,

IPR2020-01561
Patent 7,719,452 B2

that Petitioner has demonstrated by a preponderance of the evidence that the challenged claims would have been unpatentable over Fu and Lewis.

1. *Fu (Ex. 1005)*

Fu describes a 10-bit 40-Msample/s two-channel parallel pipelined analog-to-digital (ADC) with monolithic digital background calibration. Ex. 1005, 1904. The ADC consists of M ADC's in parallel, an analog demultiplexer at the input and a digital multiplexer at the output. *Id.* Each ADC operates at an overall sampling rate f_s divided by M . *Id.* During operation, the analog demultiplexer selects each ADC in turn to process the input signal. *Id.* The corresponding digital multiplexer selects the digital output of each ADC periodically and forms a high-speed ADC output. *Id.* An example ADC is illustrated in Figure 4, reproduced below.

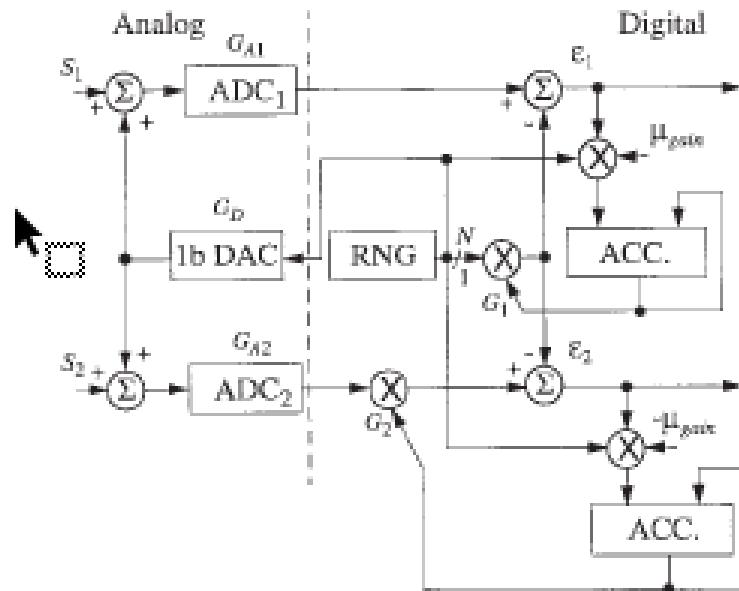


Fig. 4. Modified gain calibration system for two time-interleaved ADC's.

Figure 4, above, shows a modified gain calibration system an ADC comprising two time-interleaved ADCs. *Id.* at 1906. The ADC receives an analog signal S_1 and generates a combined digital code ε_1 . *Id.* at 1905–1907.

Figure 7, reproduced below, illustrates an example of a pipelined ADC.

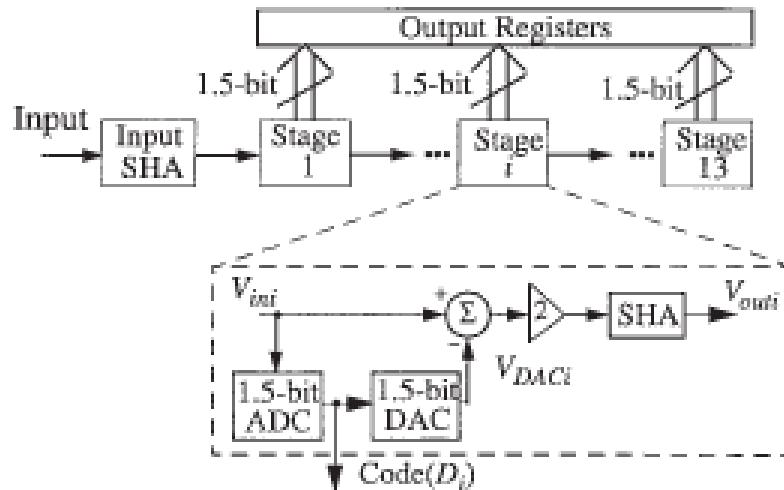


Fig. 7. Block diagram of the 14-bit pipelined ADC.

Figure 7, above, illustrates a block diagram of one pipelined ADC. *Id.* at 1907. The ADC includes a sampler (“Input SHA”) that samples an incoming analog signal (“Input”) and a plurality of signal converter stages (“Stage 1, Stage i . . . Stage 13”) that successively process the samples. *Id.* The stages process the analog samples and dither signals and generate respective digital codes (“1.5 bit”), which are fed to output registers (“Output Registers”). *Id.* at 1905.

2. *Independent Claims 1 and 13*

Petitioner argues the combination of Fu and Lewis teach or suggest the limitations of claims 1–4, 8, 9, and 13–16. Pet. 58–86. Petitioner argues that both Fu and Lewis disclose an “analog to digital converter system” as recited in claim [1A]. *Id.* at 58 (citing Ex. 1002 ¶¶ 177–179). Petitioner argues that at least Fu discloses “a sampler” for providing input signal samples as called for in claim [1B]. *Id.* at 60 (citing Ex. 1002 ¶¶ 181–182). Petitioner argues for claim [1C] that both Fu and Lewis disclose pipelined

IPR2020-01561
Patent 7,719,452 B2

signal converters for processing signal samples. *Id.* at 62–63 (citing Ex. 1002 ¶¶ 185–187). Considering claim [1D], Petitioner argues that Fu teaches “the 1b DAC is configured to ‘inject’ the dither signals into the pipelines ADC,” and “the pipelined ADC is processed by a first signal converter stage ‘Stage 1’ of the pipeline, which includes a sampler circuit ‘SHA.’” *Id.* at 66 (citing Ex. 1002 ¶ 190). Petitioner argues with respect to element [1E] that a person of ordinary skill in the art understood that Fu’s “Output Registers at least logically combine the digital codes “ D_i ” into a combined digital code.” *Id.* at 68 (citing Ex. 1002 ¶¶ 193–194). Petitioner argues for limitation [1F] that “Fu teaches multiplying the output of the random number generator “RNG” [] by a variable gain “G1” [] for subsequent subtraction from ADC1 with a differencer []. *Id.* at 72 (citing Ex. 1002 ¶¶ 198–199). For limitation [1G], Petitioner argues that “Fu’s analog dither signals will cause at least one stage of its pipelined ADC to operate at different operating points,” and that in Fu’s “time-interleaved architecture, each successive sample $x(t)$ would be processed by a different ADC (*i.e.*, ADC0 – ADCM-1).” *Id.* at 73–74 (citing Ex. 1002 ¶¶ 200–201).

Petitioner contends that Dr. Holberg identifies several different reasons why a person of ordinary skill in the art would combine the teachings of Fu and Lewis. *Id.* at 53–58 (citing Ex. 1002 ¶¶ 159–165, 229–233). Dr. Holberg testifies that “Fu discloses a pipelined signal converter stage includes a SHA, a sub-ADC, and a sub-DAC - but these elements are illustrated simply using symbols to represent their respective functions.” Ex. 1002 ¶ 159 (citing Ex. 1005, Fig. 7). Dr. Holberg testifies that these ADC components and their structural circuitry are well-known, but, “Lewis, on other hand, does provide the circuit details that a POSITA would naturally look to in order to implement the functionality disclosed by Fu.” *Id.* (citing

IPR2020-01561
Patent 7,719,452 B2

Ex. 1006, Figs 6(a) and 9). Dr. Holberg reasons that “[g]iven that the performance and function of such circuits were well known, the results of such substitution would have been predictable to a POSITA.” *Id.* ¶ 164.

Patent Owner does not expressly dispute the combination of Fu and Lewis, but argues that “neither Fu nor Lewis contains any teaching or suggestion regarding a pipelined converter in which dither propagates through all the converter stages as claimed, the combination of Fu and Lewis likewise fails to anticipate any of the challenged claims.” PO Resp. 59 (citing Ex. 2002 ¶¶ 82–83). Patent Owner argues, as it has throughout this proceeding, that due to “dither exhaustion,” there “is no basis for Petitioner’s suggestion – contrary to the ’452 patent’s teachings— that Fu’s injected signal would propagate to downstream converter stages.” *Id.* at 62 (citing Ex. 2002 ¶ 91).

We determine that Petitioner has shown that a person of ordinary skill in the art, considering the teachings in Fu, would have looked to Lewis in order to determine more specifically a circuit structure for implementing the teachings in Fu. Pet. 53–58. Petitioner explains that Lewis provides “detailed disclosure to fill in details that Fu presumably considered too well-known and/or too trivial to provide.” Pet. 53 (citing Ex. 1002 ¶ 159). Dr. Holberg testifies that in view of the level of ordinary skill in the art “[b]ecause such details are not necessary to understand the invention disclosed by Fu, presumably, they were omitted. Lewis, on other hand, does provide the circuit details that a POSITA would naturally look to in order to implement the functionality disclosed by Fu.” Ex. 1002 ¶ 159 (citing Ex. 1006, Figs 6(a) and 9). Dr. Holberg’s testimony is essentially unrebutted on this point. Dr. Holberg also offers several rationales explaining why a person of ordinary skill in the art would have combined Fu and Lewis. Dr.

IPR2020-01561
Patent 7,719,452 B2

Holberg testifies, for example that like Fu, Lewis “discloses at the system level a pipelined ADC system employing similar components. . .

[a]dditionally, Lewis discloses the details regarding, *e.g.*, basic switched capacitor circuit implementations for some of the components. *Id.* ¶ 162 (citing Ex. 1006, Figs. 6(a), 9; pgs. 957–959). Dr. Holberg explains persuasively that a person of ordinary skill in the art would have known to substitute or use Lewis’s disclosed circuit structures with Fu’s higher level disclosure because Lewis’s “circuits are basic building blocks for analog circuits and are readily substituted for one for another. Given that the performance and function of such circuits were well known, the results of such substitution would have been predictable to a POSITA.” *Id.* ¶ 164. Patent Owner and Dr. Moon do not expressly dispute Dr. Holberg’s testimony as to the rationale to combine and we are persuaded that a person of ordinary skill in the art would have been motivated to look to Lewis in order to determine more specific circuit structures to carry out the more functional teachings in Fu.

We turn next to the parties’ express arguments and evidence pertaining to the teachings of Fu and Lewis as they relate to independent claims 1 and 13.

Patent Owner again relies on its erroneous claim construction “that the analog input signals be processed along ‘different signal-processing paths’ of *each* of the *multiple* signal converters in the analog-to-digital converter.” *Id.* at 63. As discussed above, we do not find this argument persuasive because the claims do not require that the dither portion of the combined sampled input signals propagates through all, or each, stage of the converter system. Section II. G. Patent Owner next argues that Fu “show[s] the addition of a random analog value using **summing nodes** located *before* the

IPR2020-01561
Patent 7,719,452 B2

pipelined ADC stages,” and thus does not inject a dither signal into a converter stage as required by independent claims [1D] and [13C]. *Id.* at 61 (citing Ex/ 2002 ¶ 89).

In light of Patent Owner’s second argument here, we address the following question.

a) Whether Fu teaches injecting dither signals “into at least a selected one of said signal converters”

Patent Owner argues specifically that “Fu teaches injecting a random signal into a converter system at a point **before** an ADC pipeline, and not **into** a converter stage of an ADC pipeline. PO Resp. 64 (citing Ex. 2002 ¶ 96). Patent Owner asserts that a diagram provided by Petitioner, ostensibly combining Fu’s Figures 4 and 7, and alleged to show injection of dither signal into a first pipelined stage “was **fabricated** by Petitioner and is **not** found anywhere in Fu. In fact, the **actual** diagrams in Fu clearly show that the SHA prior to the first stage is separate from the first signal converter stage of the ADC pipeline.” *Id.* at 65–66.

Petitioner responds, arguing that Patent Owner’s argument “fails to recognize how a POSITA would understand the prior art.” Reply 19 (citing *KSR*, 550 U.S. 398. Petitioner contends that Patent Owner’s argument is mainly based on Fu’s figure 4, for example, as reproduced below, depicting a summer, or adder, illustrated prior to the ADC.

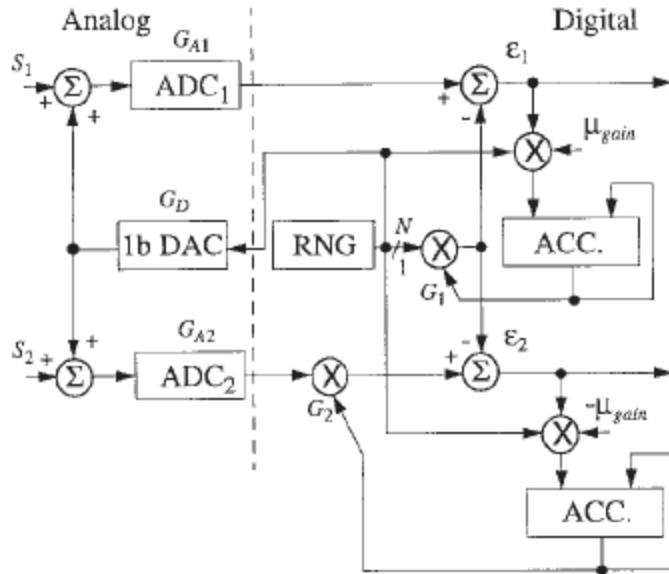


Fig. 4. Modified gain calibration system for two time-interleaved ADC's.

Figure 4 illustrates a random number generator RNG applying dither via 1b DAC to an input signal S_1 . Petitioner argues that Patent Owner's argument is a narrow reading of Fu's disclosure and teaching, and Petitioner relies on Dr. Holberg, who explains that "Fu's adder is symbolically represented for clarity of illustration, and . . . simply represents the *function* of combining signals (such as the dither signal and the analog input signal), *e.g.*, by applying the two signals onto a common capacitor or capacitors." Reply 19 (citing Ex. 1002 ¶ 220).

For Patent Owner, Dr. Moon testifies that according to Figure 4, "Fu adds a random signal to the analog signal that is input into an ADC pipeline, not into a signal converter stage of the ADC pipeline." Ex. 2002 ¶ 97. In other words, Dr. Moon's point is that "Fu clearly injects its random analog signal upstream of the ADC pipeline, and not into any signal converter stage of the pipeline." *Id.*

Considering the level of ordinary skill in the art, we find Dr. Holberg's testimony more persuasive. Considering Figure 4, above, Fu

IPR2020-01561
Patent 7,719,452 B2

discloses functionally, (as opposed to structurally with a specific circuit) combining a dither signal from 1b DAC with input signal S_1 and entering into ADC_1 . We acknowledge that Figure 4 illustrates diagrammatically summing the digital signal and then sending it to ADC_1 , but Dr. Holberg explains persuasively that a person of ordinary skill in the art would understand that dither is injected into Stage 1 of the ADC_1 by combining it with the input signal S_1 , and then providing that signal to a sampler circuit, SHA, for Stage 1 of Fu. Dr. Holberg testifies that Fu's "combining function is a form of injecting, and thus Fu teaches the 1b DAC is configured to 'inject' the dither signals into the pipelined ADC." Ex. 1002 ¶ 190. Dr. Holberg summarizes that a person of ordinary skill in the art would have understood "Fu's b1 DAC thus 'inject[s]' the analog dither signals into the 'signal converters'... which as noted above, each contain a sampler." *Id.*

Although Patent Owner argues that Fu's Figures 4 and 7 have been altered and misrepresent Fu teachings, considering the level of ordinary skill in the art, we find Patent Owner and Dr. Moon's analysis of Fu too narrow. PO Resp. 65–66. We are persuaded by Dr. Holberg's testimony that a person of skill in the art would have understood Fu in a similar manner to Petitioner's combination of Fu's Figures 4 and 7, reproduced below.

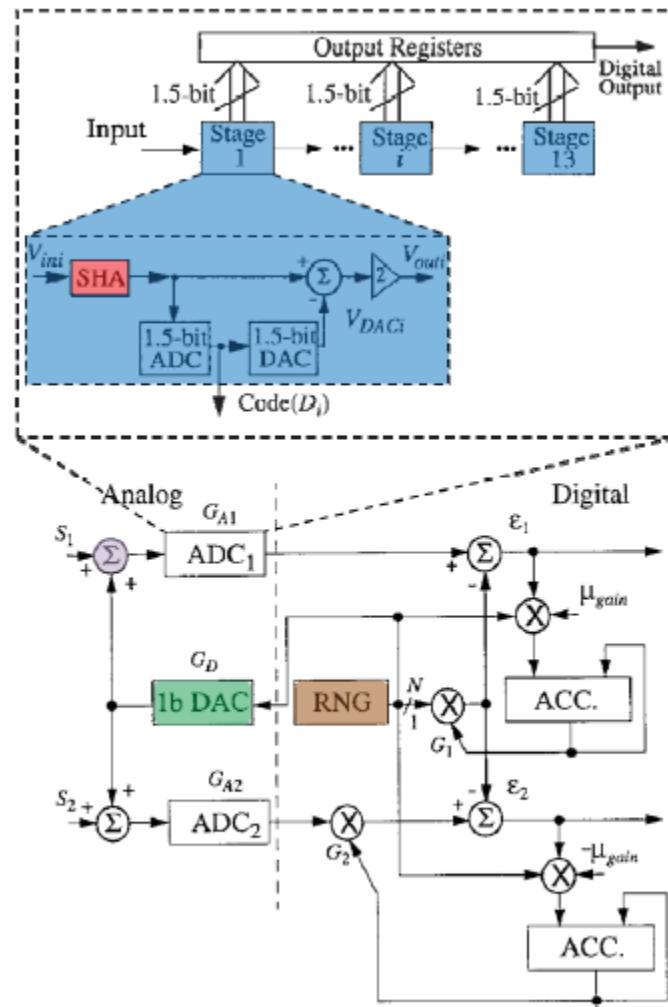


Figure C (combined teachings of Fu Figs. 4 and 7).

Petitioner's combination of the teachings in Fu's Figures 4 and 7 is reproduced above, and illustrates injecting dither, combined with the input signal, into a sampler circuit of Stage 1 in Fu. Pet. 67. Fu's Figure 7 depicts each Stage of its pipelined signal converter including a sampler circuit SHA. Ex. 1005, 1907, Figure 7; *see also* Ex. 1002 ¶ 184 (Dr. Holberg testifying that “[a] POSITA would recognize that a S/H circuit samples an incoming signal and provides samples of that signal to circuitry at its output.”). Considering all the evidence before us, including the competing testimony of Dr. Moon and Dr. Holberg, we are persuaded that a person of ordinary skill

IPR2020-01561
Patent 7,719,452 B2

in the art would have understood that Fu, as a whole, and considering the level of ordinary skill in the art, teaches “inject[ing] analog dither signals into at least a selected one of [said sampler and] said signal converters which process said samples and said analog dither signals into a plurality of digital codes,” as called for in independent claims 1 and 13.

Having considered the entire record now before us, including the arguments and evidence presented by both parties, we are persuaded by Petitioner’s arguments and evidence that claims 1 and 13 would have been obvious over Fu and Lewis.

3. Dependent claims 2–4, 8, 9, and 14–16

Petitioner argues that Fu discloses a pseudorandom number generator providing a random digital code to the DAC, as well as a differencer as called for in claim 2. Pet. 76–77. Petitioner argues for claim 3 that a person of ordinary skill in the art would have understood that dither is added via a sampler circuit into each of Fu’s converter stages. *Id.* at 77–78 (citing Ex. 1002 ¶ 208).

For claim 4, Petitioner argues that Fu discloses using 25% of signal amplitude for dither which is less than the output signal window of the converter stages *Id.* at 79–80 (citing Ex. 1002 ¶ 210). Petitioner argues that the limitations of claim 8 are similar to those of claim [1D] and “in Fu, the analog dither signal output from the DAC is injected into the sampler ‘SHA,’ which is part of the first converter stage ‘Stage 1.’” *Id.* at 80 (citing Ex. 1002 ¶¶ 211–212). Petitioner argues that claim 9, which depends from claim 8, is similar to claim 4 and that Fu discloses a dither range, e.g., 25% of the signal amplitude which is less than the full output signal window. *Id.* at 82 (citing Ex. 1002 ¶ 215). For claims 14, 15, and 16, which ultimately depend from independent claim 13, Petitioner argues these claims are

IPR2020-01561
Patent 7,719,452 B2

substantively the same as claims 2, 8 and 9 and therefore obvious over Fu and Lewis for the same reasons as previously discussed. *Id.* at 86 (citing Ex. 1002 ¶¶ 226–228).

Patent Owner argues that these dependent claims would not have been obvious for the same reasons as the respective independent claims 1 and 13, from which they depend. PO Resp. 67. Patent Owner offers no substantive rebuttal arguments or testimony contradicting that of Petitioner and Dr. Holberg as to these dependent claims. *Id.* Having considered the entire record now before us, including the arguments and evidence presented by both parties, we adopt and incorporate Petitioner’s showing as to claims 2–4, 8, 9, and 14–16, as set forth in the Petition and summarized above, as our own. *See* Pet. 76–82, 86. Accordingly, we are persuaded by Petitioner’s arguments and evidence that claims 2–4, 8, 9, and 14–16 would have been obvious over Fu and Lewis.

4. Conclusion as to Obviousness Based on Fu and Lewis

Based on the complete trial record in the proceeding, for the reasons above we are persuaded that claims 1–4, 8, 9, and 13–16 would have been obvious in view of Fu and Lewis. Because, together with the challenges based on Cesura, as well as Cesura, Lewis, and Bjornsen, we determine that all the challenged claims of the ’452 patent are unpatentable and we do not reach Petitioner’s challenge asserting that claims 12, 19, and 20 would have been obvious based on Fu, Lewis, and Bjornsen.

III. CONCLUSION

As summarized in the table below, the Petition and supporting evidence has shown by a preponderance of the evidence that claims 1–4, 8, 9, 12–16, 19, and 20 of the '452 patent would have been obvious.⁸

Claims	35 U.S.C. §	Reference(s)/ Basis	Claims Shown Unpatentable	Claims Not Shown Unpatentable
1, 2, 8, 9, 13–16	103	Cesura	1, 2, 8, 9, 13–16	
12, 19, 20	103	Cesura, Lewis, and Bjornsen	12, 19, 20	
1–4, 8, 9, 13–16	103	Fu and Lewis	1–4, 8, 9, 13–16	
12, 19, 20	103 ⁹	Fu, Lewis, and Bjornsen		
Overall Outcome			1–4, 8, 9, 12–16, 19, 20	

⁸ Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner's attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding*. See 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. See 37 C.F.R. § 42.8(a)(3), (b)(2).

⁹ As explained above, because we determined that all the challenged claims of the '452 patent are unpatentable based on the other grounds, we do not reach Petitioner's challenge asserting that claims 12, 19, and 20 would have been obvious based on Fu, Lewis, and Bjornsen.

IPR2020-01561
Patent 7,719,452 B2

IV. ORDER

For the reasons given, it is

ORDERED that, based on a preponderance of the evidence claims 1–4, 8, 9, 12–16, 19, and 20 of the '452 patent have been shown to be unpatentable; and

FURTHER ORDERED that, because this is a Final Written Decision, any party to the proceeding seeking judicial review of this Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

IPR2020-01561
Patent 7,719,452 B2

PETITIONER:

Mehran Arjomand
Jean Nguyen
Richard Hung
Alex Yap
Hector Gallegos
MORRISON & FOERSTER LLP
marjomand@mofo.com
jnguyen@mofo.com
rhung@mofo.com
ayap@mofo.com
hgallegos@mofo.com

David Fehrman
DSA LEGAL SOLUTIONS PC
dfehrman@dsa-legal.com

PATENT OWNER:

Peter Dichiara
Scott Bertulli
Cynthia Vreeland
Brian J. Lambson
WILMER CUTLER PICKERING
HALE AND DORR, LLP
peter.dichiara@wilmerhale.com
scott.bertulli@wilmerhale.com
cynthia.vreeland@wilmerhale.com
Brian.lambson@wilmerhale.com

Michael Diener
Claire Rollor
ANALOG DEVICES, INC.
Michael.Diener@analog.com
Claire.Rollor@analog.com

IPR2020-01561
Patent 7,719,452 B2

(12) **United States Patent**
Bardsley et al.

(10) Patent No.: US 7,719,452 B2
(45) Date of Patent: May 18, 2010

(54) PIPELINED CONVERTER SYSTEMS WITH ENHANCED LINEARITY

(75) Inventors: **Scott Gregory Bardsley**, Gibsonville, NC (US); **Bryan Scott Puckett**, Stokesdale, NC (US); **Michael Ray Elliott**, Summerfield, NC (US); **Ravi Kishore Kummaraguntla**, Austin, TX (US); **Ahmed Mohamed Abdelatty Ali**, Oak Ridge, NC (US); **Carroll Clifton Speir**, Pleasant Garden, NC (US); **James Carroll Camp**, Greensboro, NC (US)

(73) Assignee: **Analog Devices, Inc.**, Norwood, MA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 118 days.

(21) Appl. No.: 12/284,672

(22) Filed: Sep. 23, 2008

(65) **Prior Publication Data**

US 2010/0073210 A1 Mar. 25, 2010

(51) **Int. Cl.**
H03M 1/20 (2006.01)

(52) **U.S. Cl.** 341/131; 341/118; 341/120;
341/155; 341/161; 341/162

(58) **Field of Classification Search** 341/118-122,
341/131, 155, 161, 162

(56) References Cited

U.S. PATENT DOCUMENTS

6.373.424 B1* 4/2002 Soenen 341/161

6,404,364	B1 *	6/2002	Fetterman et al.	341/131
6,456,223	B1 *	9/2002	Yu et al.	341/161
6,734,818	B2 *	5/2004	Galton	341/161
6,784,814	B1 *	8/2004	Nair et al.	341/118
7,006,028	B2 *	2/2006	Galton	341/155
7,034,736	B1 *	4/2006	Ali	341/162
7,035,756	B2 *	4/2006	Maloberti et al.	702/126
7,107,175	B2 *	9/2006	Maloberti et al.	702/126
7,187,310	B2 *	3/2007	El-Sankary et al.	341/120
7,535,391	B1 *	5/2009	Newman et al.	341/131
7,602,324	B1 *	10/2009	Huang et al.	341/131
2006/0227052	A1 *	10/2006	Tavassoli	343/700 MS

* cited by examiner

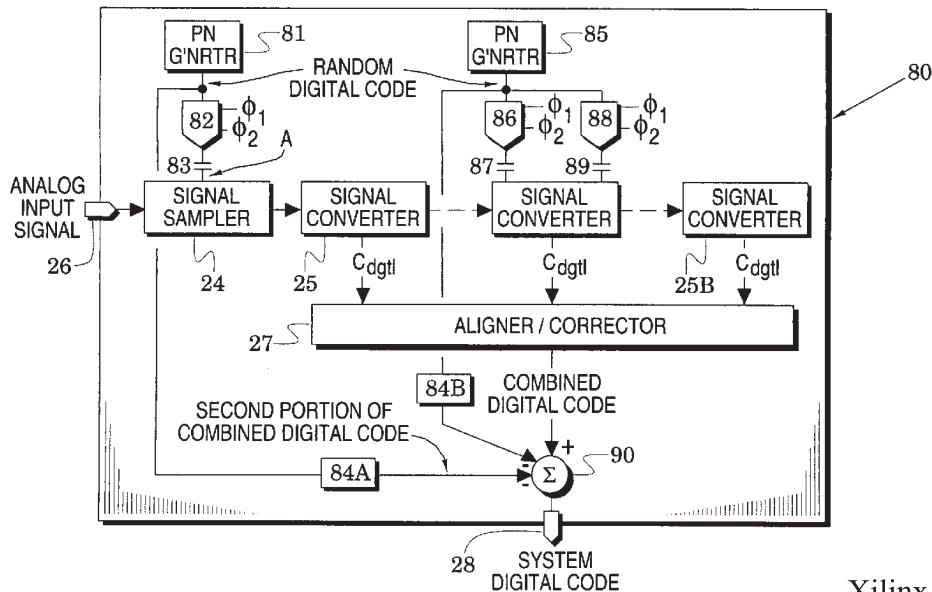
Primary Examiner—Linh V Nguyen

(74) *Attorney, Agent, or Firm*—Koppel, Patrick, Heybl & Dawson

(57) **ABSTRACT**

Signal converter system embodiments are provided to substantially reduce symmetrical and asymmetrical conversion errors. Signal-processing stages of these embodiments may include a signal sampler in addition to successively-arranged signal converters. In system embodiments, injected analog dither signals are initiated in response to a random digital code. They combine with a system's analog input signal and the combined signal is processed down randomly-selected signal-processing paths of the converter system to thereby realize significant improvements in system linearity. Because these linearity improvements are realized by simultaneous processing of the input signal and the injected dither signal, a combined digital code is realized at the system's output. A first portion of this combined digital code corresponds to the analog input signal and a second portion corresponds to the injected analog dither signal. The final system digital code is realized by subtracting out the second portion with a back-end decoder that responds to the random digital code.

20 Claims, 11 Drawing Sheets



Xilinx Exhibit 1001

U.S. Patent

May 18, 2010

Sheet 1 of 11

US 7,719,452 B2

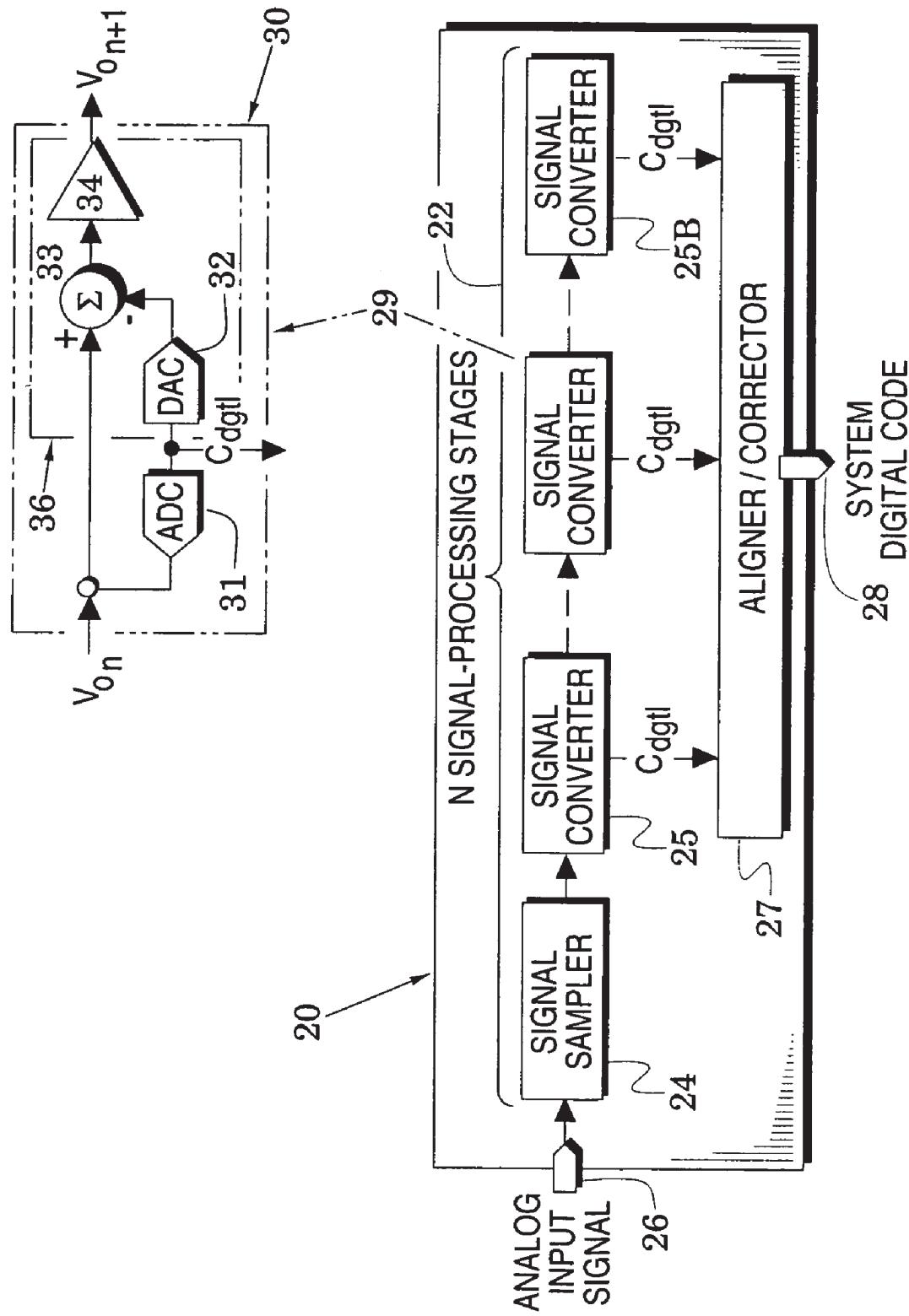


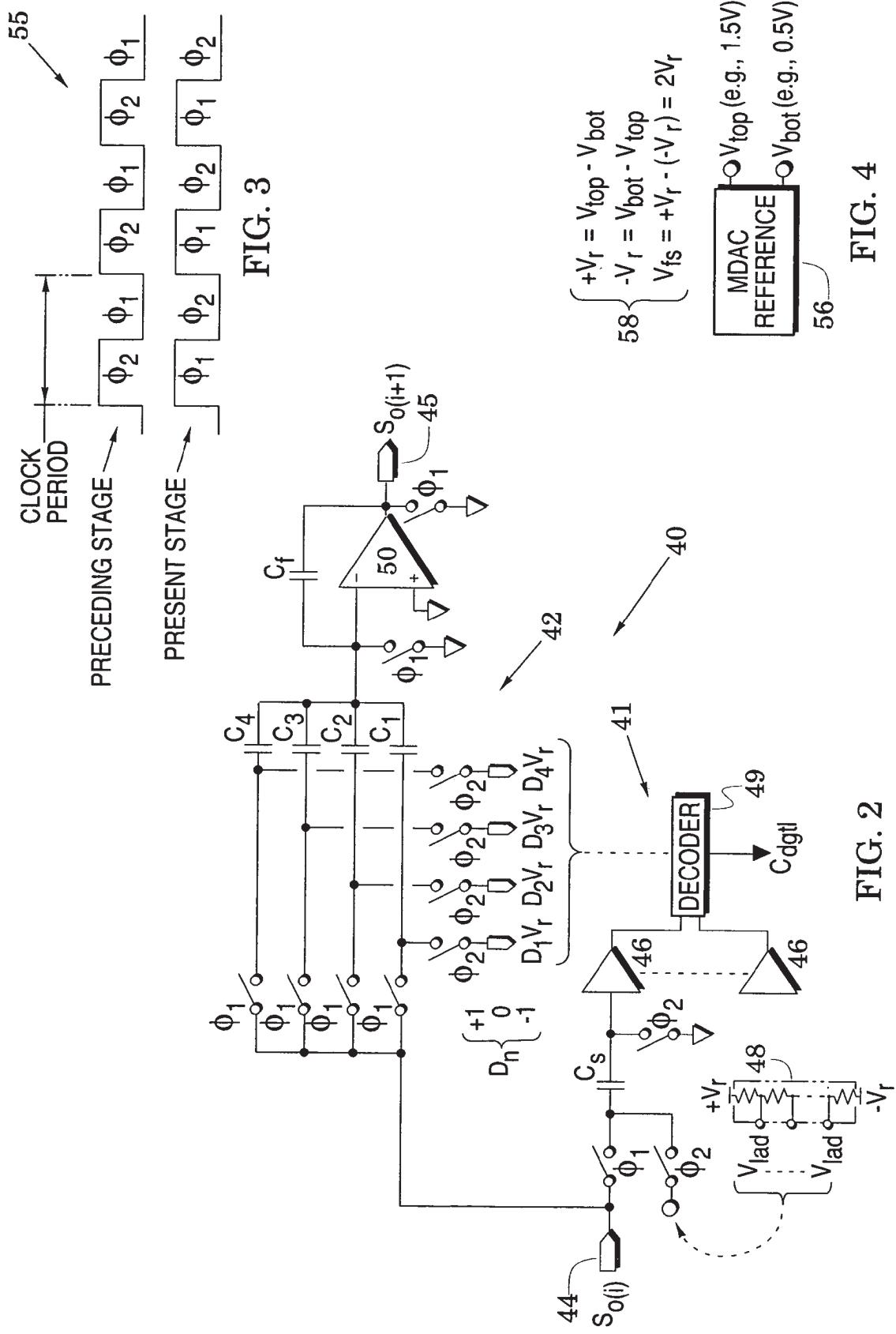
FIG. 1

U.S. Patent

May 18, 2010

Sheet 2 of 11

US 7,719,452 B2



U.S. Patent

May 18, 2010

Sheet 3 of 11

US 7,719,452 B2

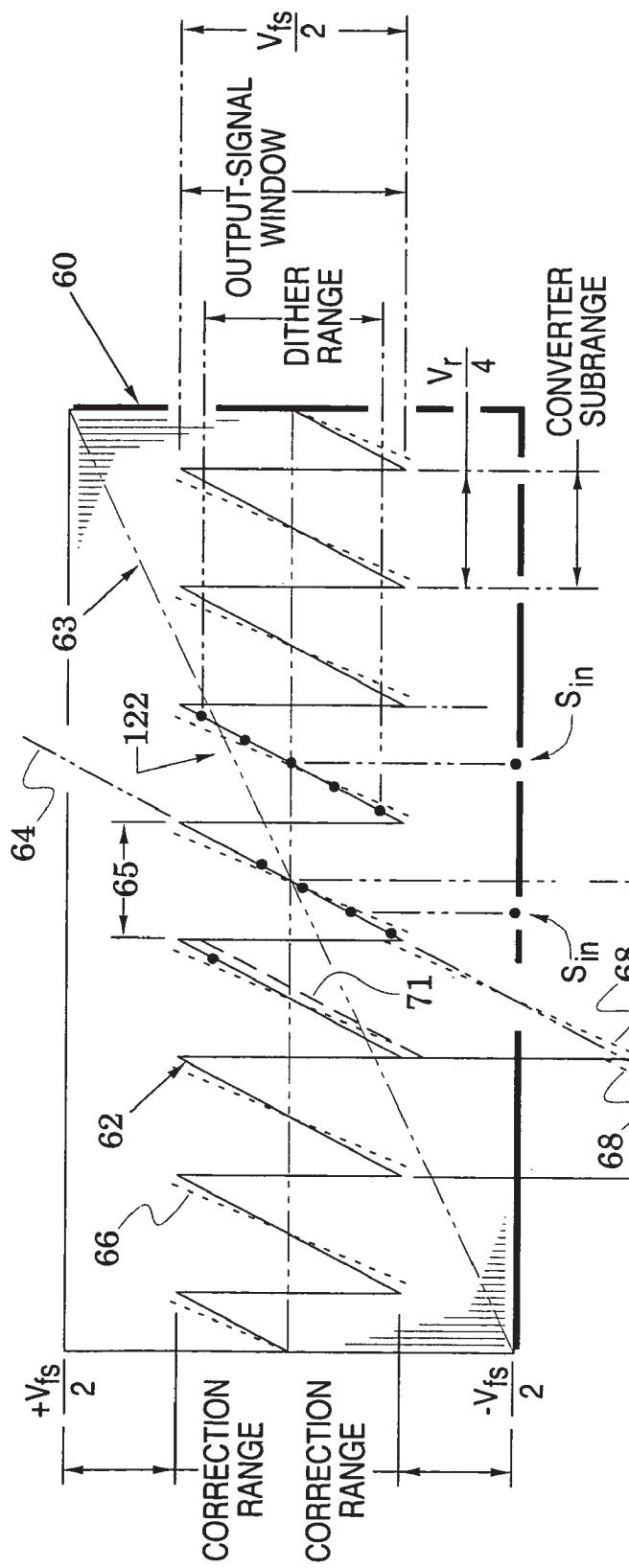
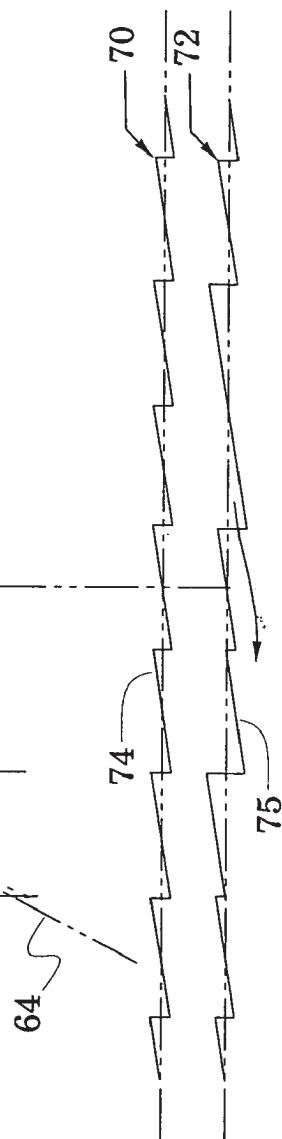


FIG. 5



U.S. Patent

May 18, 2010

Sheet 4 of 11

US 7,719,452 B2

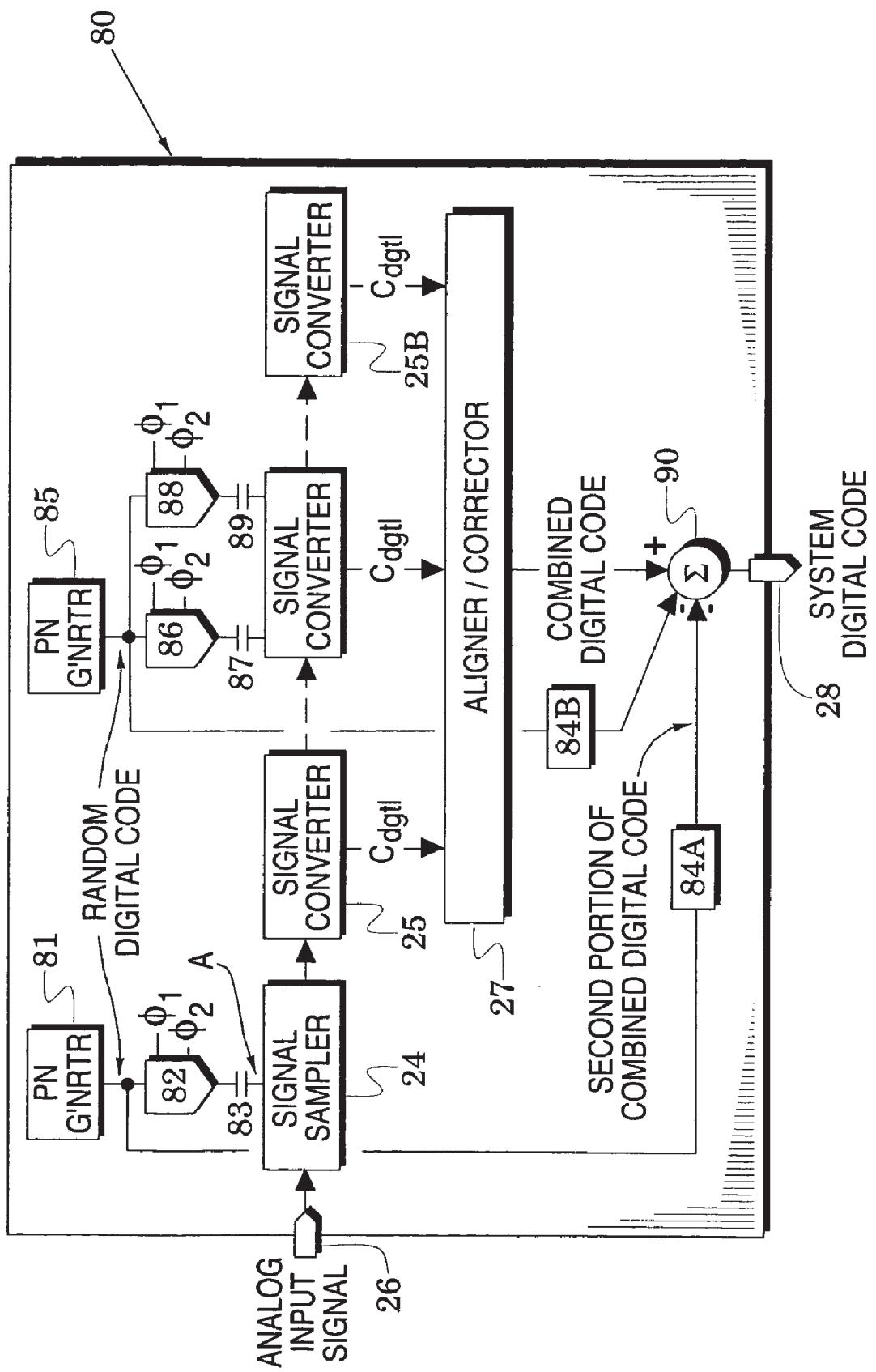


FIG. 6

U.S. Patent

May 18, 2010

Sheet 5 of 11

US 7,719,452 B2

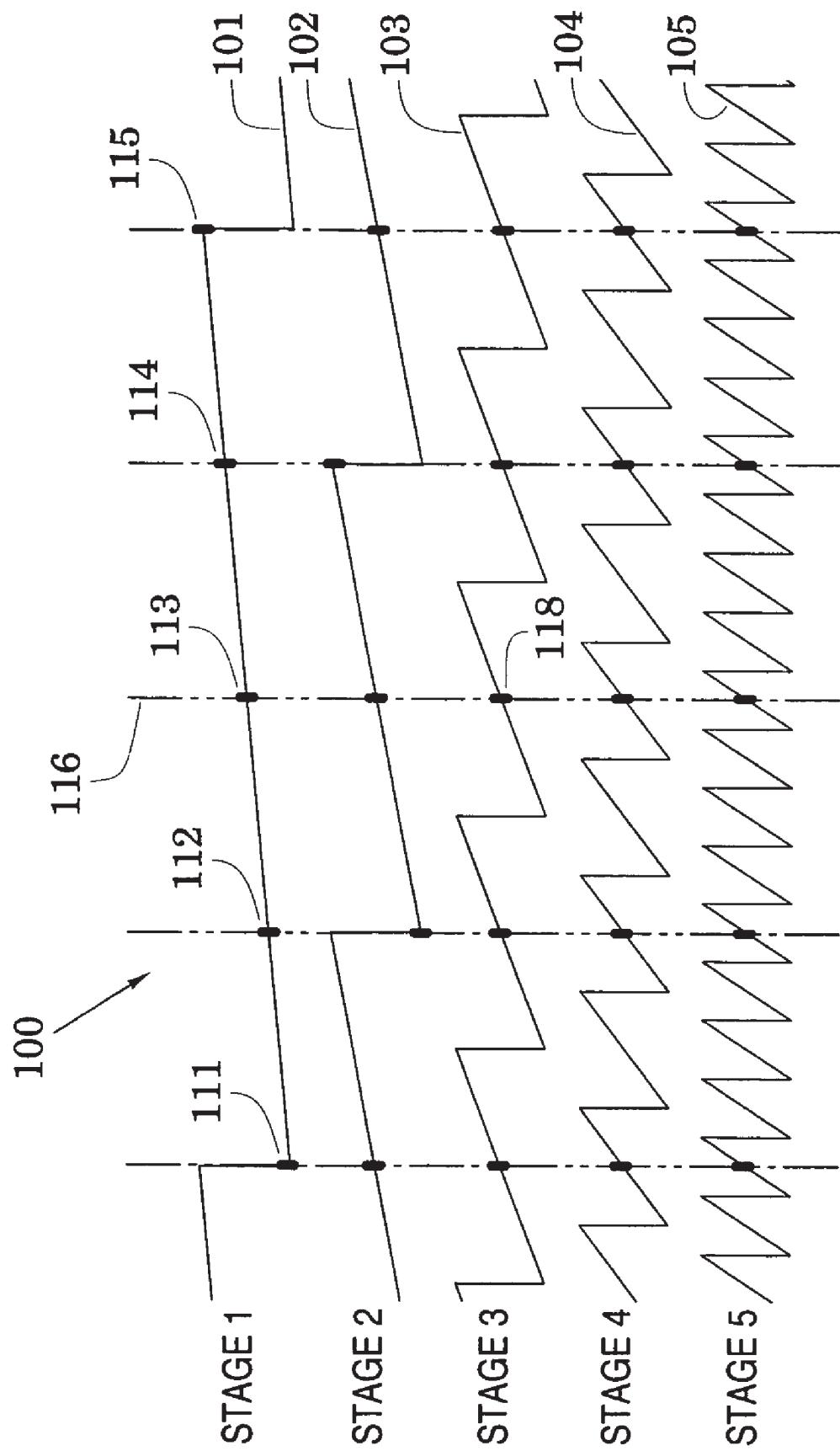


FIG. 7A

U.S. Patent

May 18, 2010

Sheet 6 of 11

US 7,719,452 B2

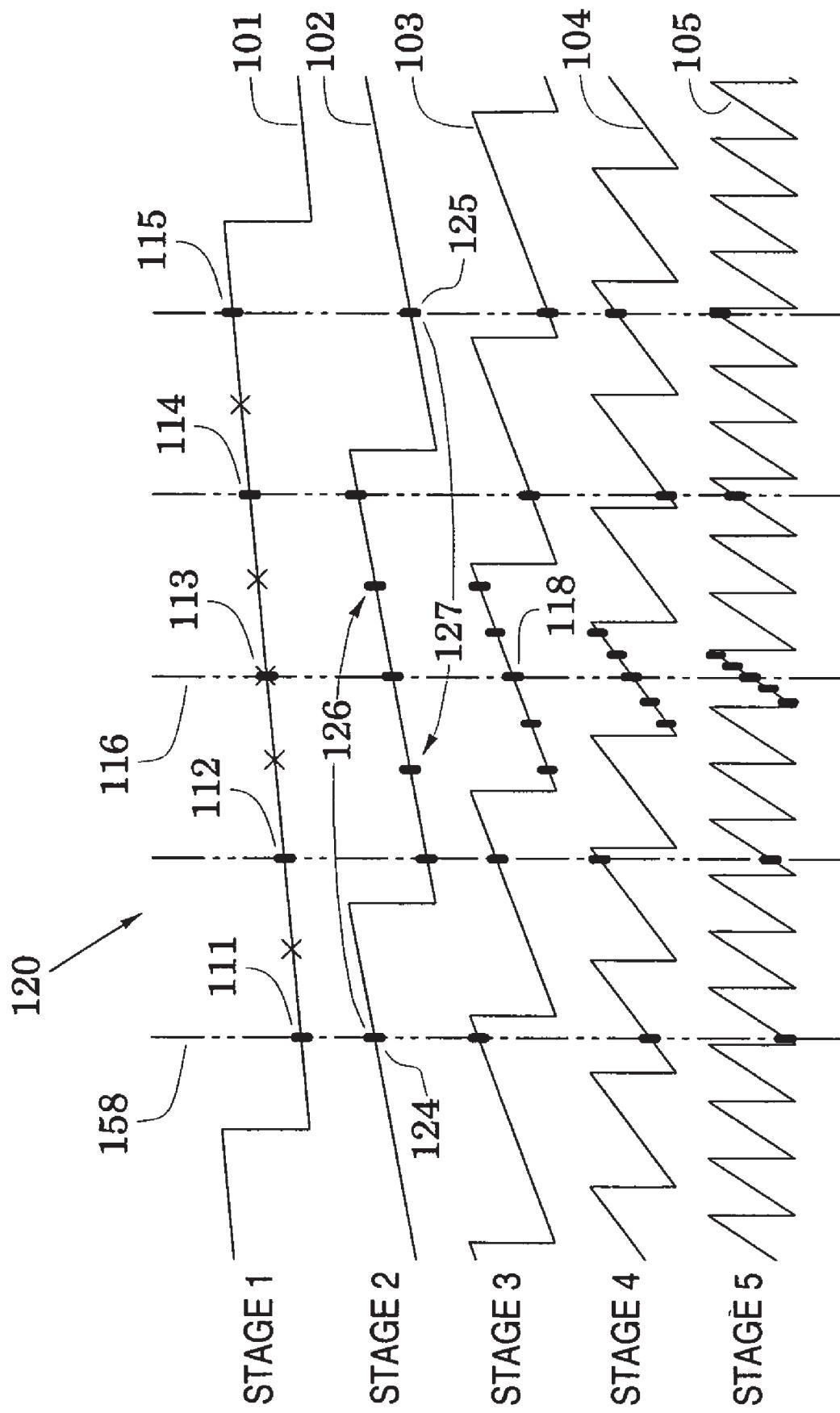


FIG. 7B

U.S. Patent

May 18, 2010

Sheet 7 of 11

US 7,719,452 B2

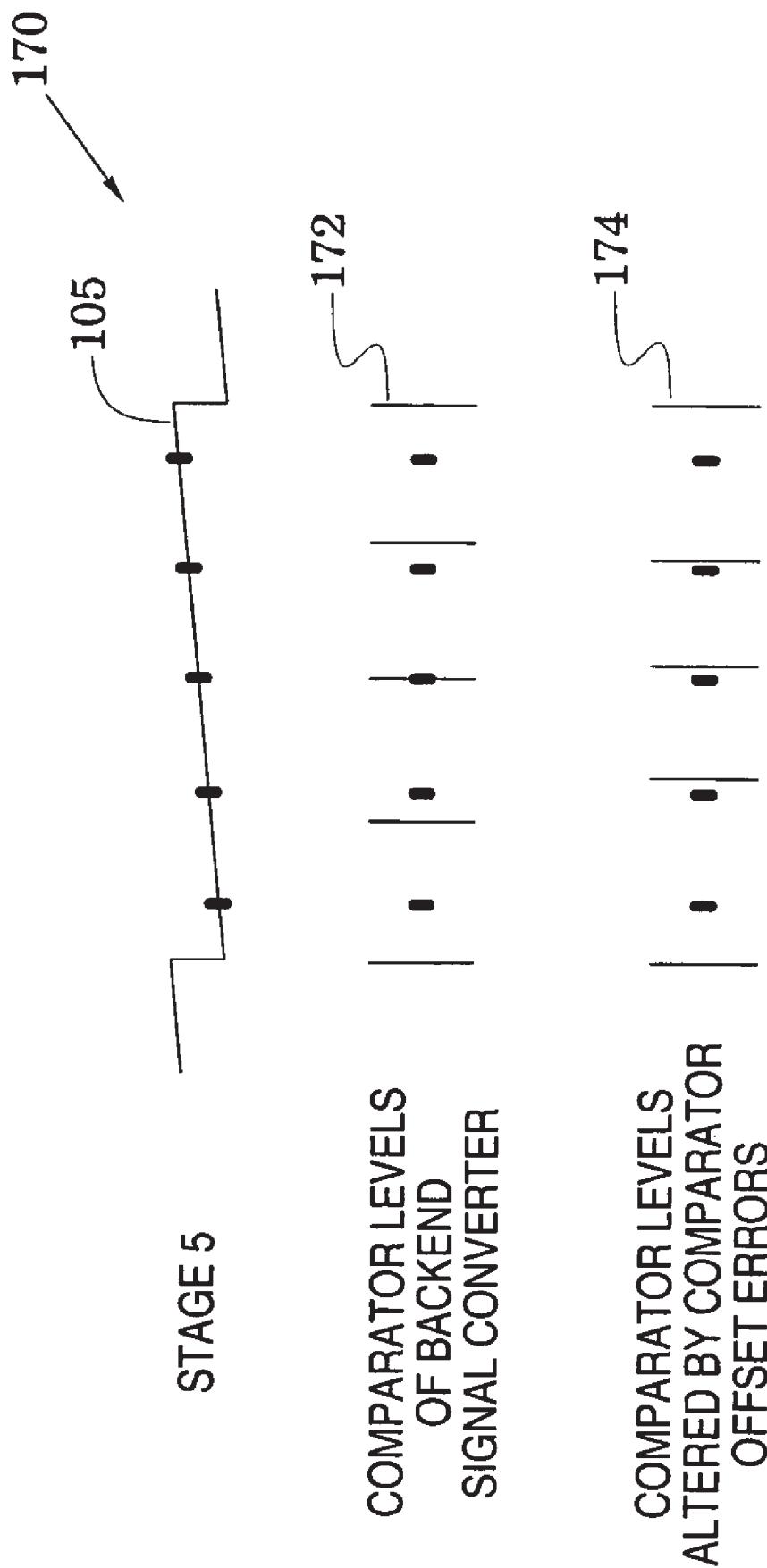


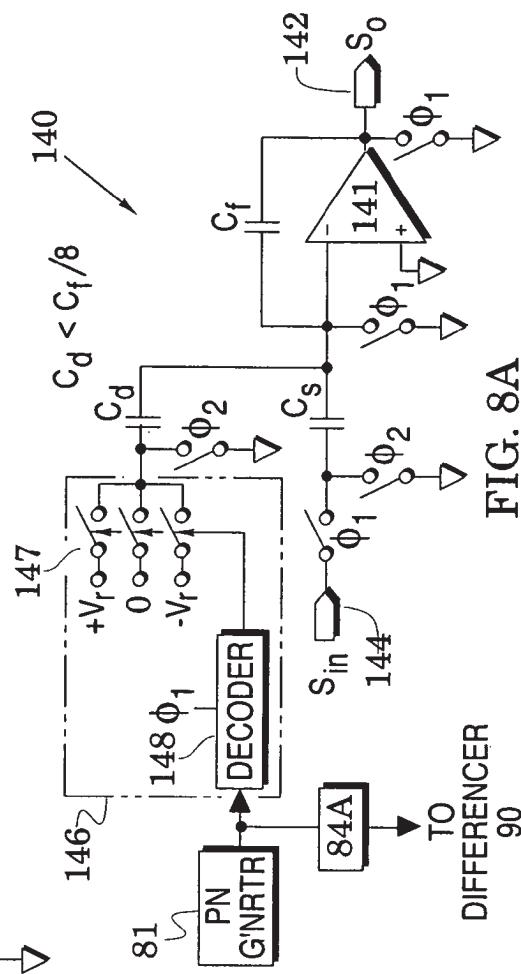
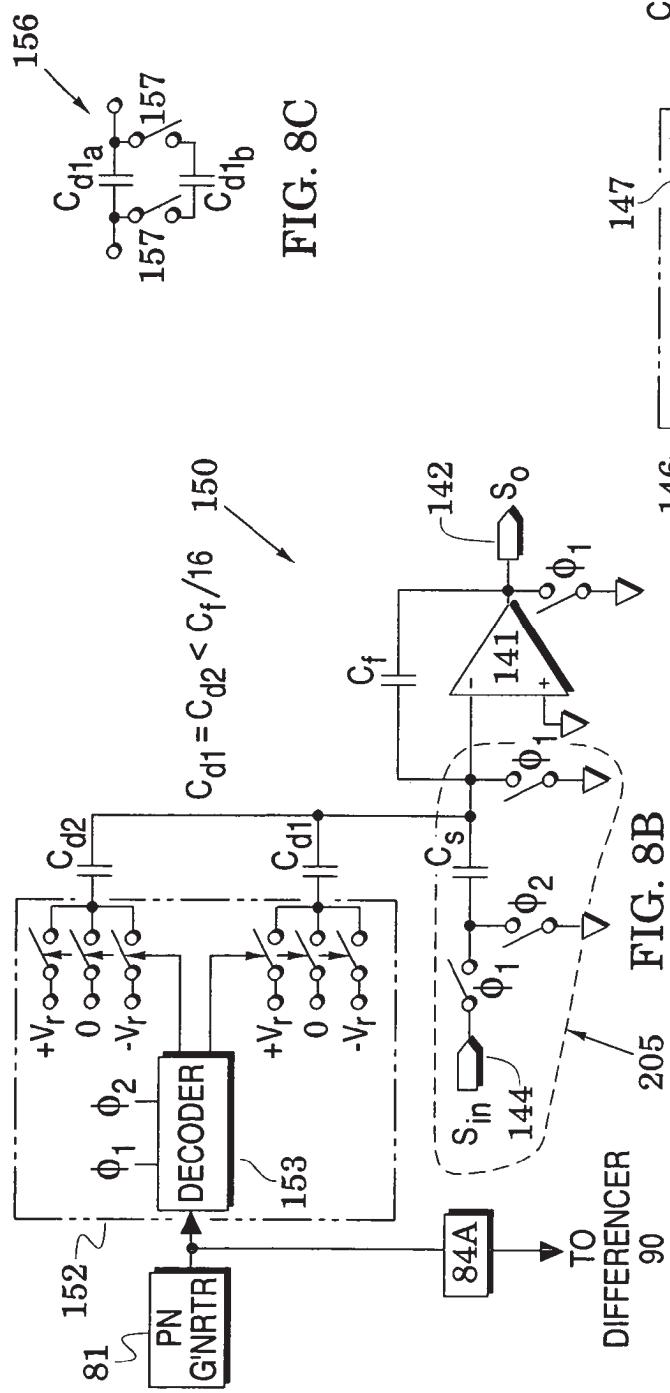
FIG. 7C

U.S. Patent

May 18, 2010

Sheet 8 of 11

US 7,719,452 B2



U.S. Patent

May 18, 2010

Sheet 9 of 11

US 7,719,452 B2

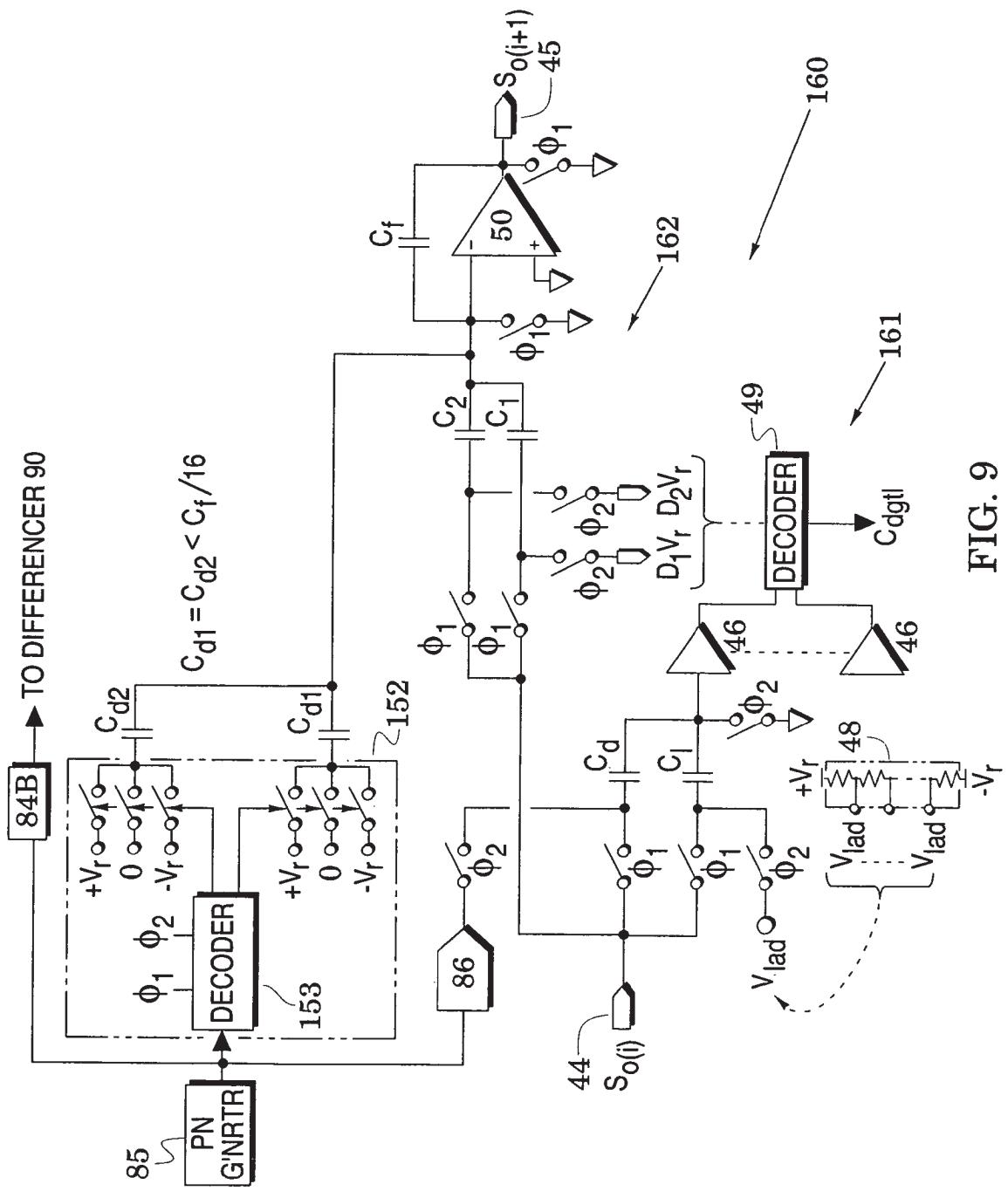


FIG. 9

U.S. Patent

May 18, 2010

Sheet 10 of 11

US 7,719,452 B2

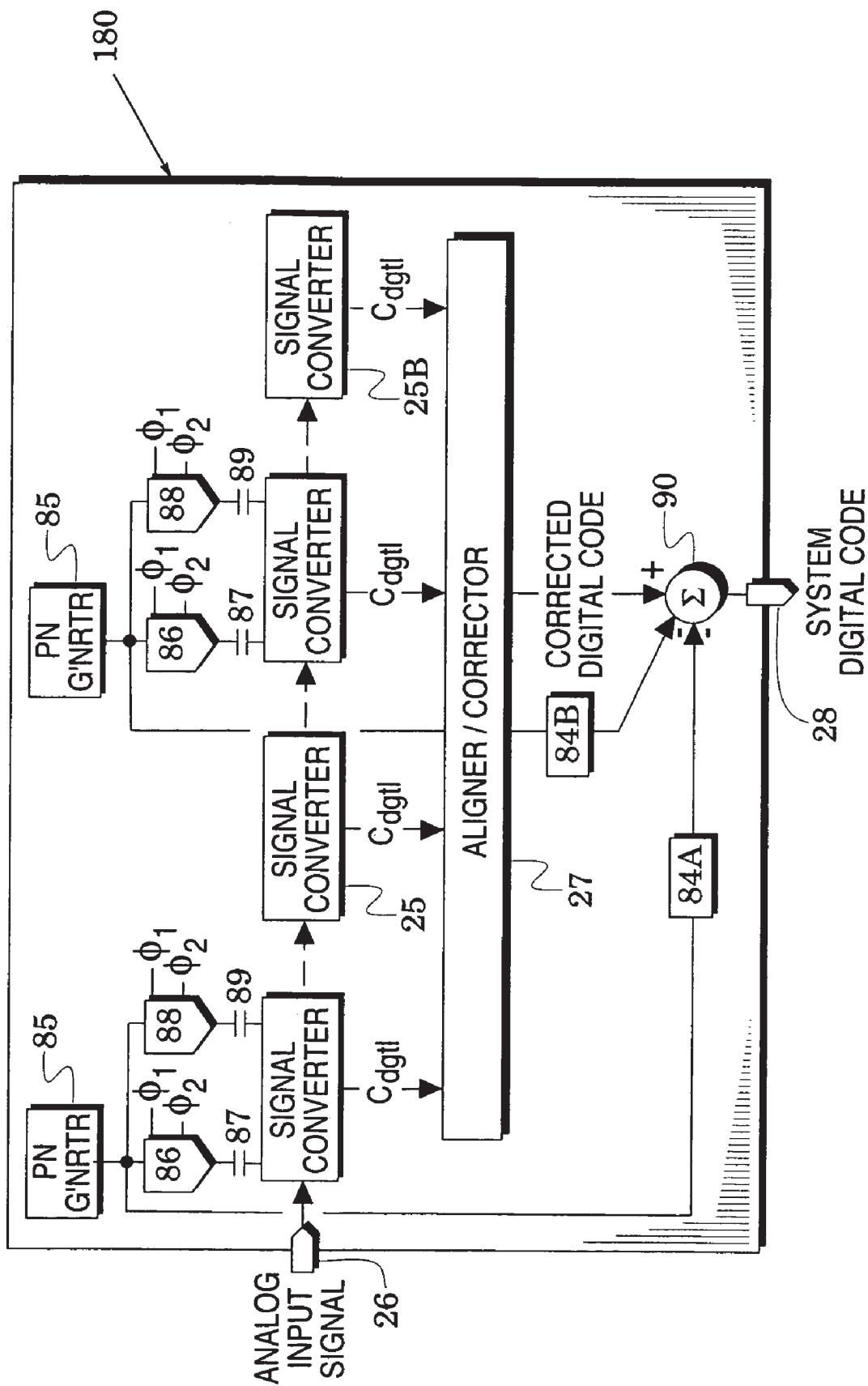


FIG. 10

U.S. Patent

May 18, 2010

Sheet 11 of 11

US 7,719,452 B2

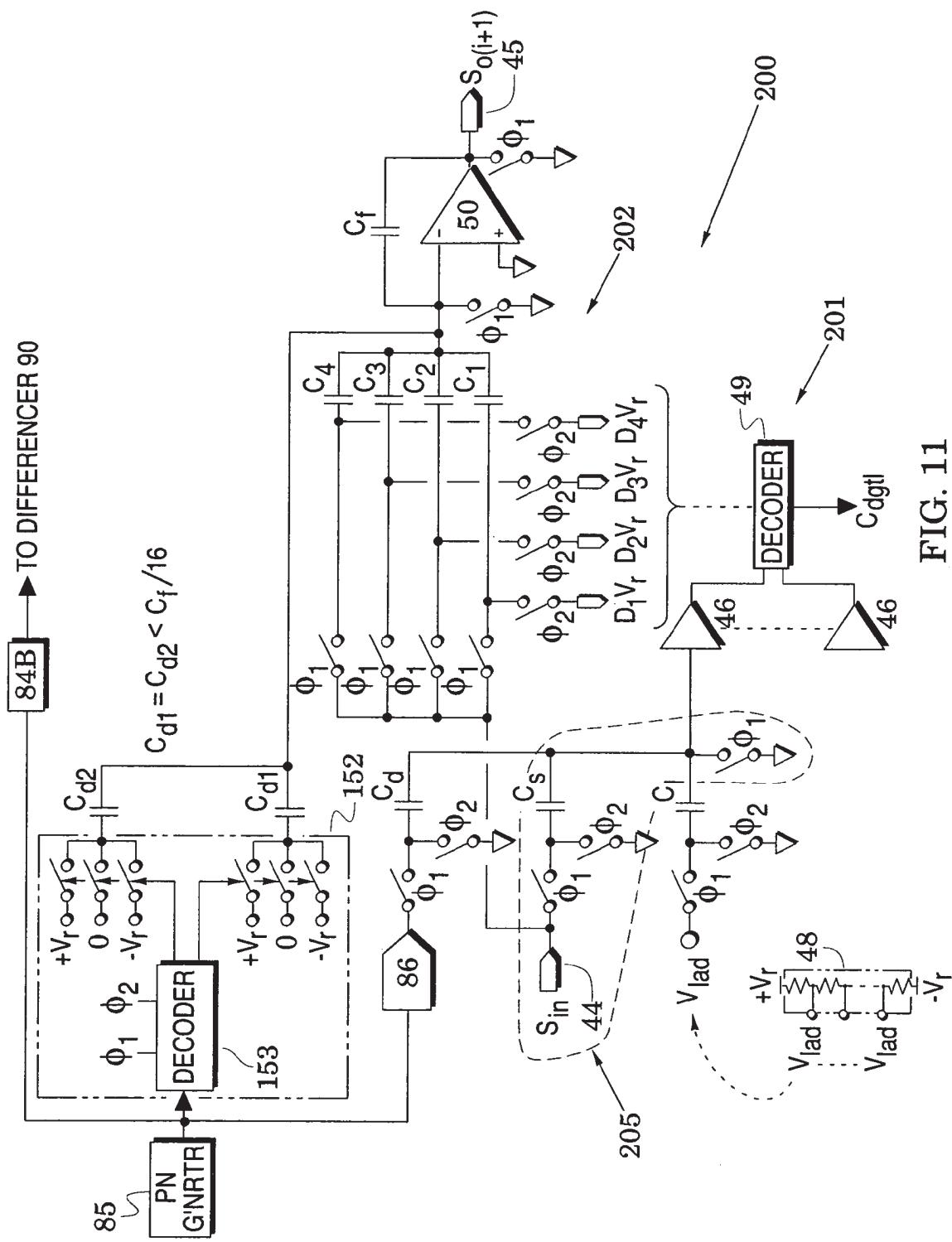


FIG. 11

US 7,719,452 B2

1

PIPELINED CONVERTER SYSTEMS WITH ENHANCED LINEARITY

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present disclosure relates generally to pipelined signal converters.

2. Description of the Related Art

Pipelined analog-to-digital signal converter systems are often used in high-speed, high-resolution conversion applications. These systems generally realize a desired number of conversion bits with a cascade (i.e., a pipeline) of lower-resolution converter stages and thus achieve high resolution at sampling speeds that are difficult to realize with other converter systems. Each stage of a pipelined system quantizes that stage's input signal to a predetermined number of digital bits and forms an analog output signal which is presented to a succeeding stage for further signal processing.

The advantages of sampling speed may, however, be negated if conversion linearity is insufficient. For example, the multistage structure of pipelined converter systems causes certain portions of the converter structure to be used repetitively as an analog input signal is swept over the system's input range and converter nonlinearity in these portions can significantly degrade the conversion of low-level dynamic signals.

Conversion linearity is generally characterized with a variety of linearity parameters such as differential nonlinearity (DNL), integral nonlinearity (INL), signal-to-noise ratio (SNR), signal-to-noise-and-distortion ratio (SINAD), and spurious free dynamic range (SFDR). DNL error indicates the difference between an actual step width of a least-significant bit and the ideal value while INL error measures the deviation of an actual transfer function from a straight line. SNR \square is computed by taking the ratio of the rms signal to the rms noise wherein the noise includes all spectral components minus the fundamental, the first four harmonics, and the DC offset. SINAD is the ratio (in dB) of the signal power to the power of all spectral components minus the fundamental and the DC offset. Finally, SFDR is the ratio of the fundamental component to the rms value of the next-largest spurious component (excluding DC offset).

Although a variety of linearizing techniques have been proposed for pipelined converter systems, increasing demands on these systems continue to exert a need for further improvements in linearity.

BRIEF SUMMARY OF THE INVENTION

The present disclosure is generally directed to pipelined converter systems with enhanced linearity. The drawings and the following description provide an enabling disclosure and the appended claims particularly point out and distinctly claim disclosed subject matter and equivalents thereof.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a diagram of a pipelined converter system;

FIG. 2 is a diagram of a signal converter embodiment in the system of FIG. 1;

FIG. 3 is a diagram of clock signals for use in the signal converter of FIG. 2;

FIG. 4 is a reference signal generator which may be used in the system of FIG. 1;

FIG. 5 is a transfer-function diagram that corresponds to the signal converter of FIG. 2;

2

FIG. 6 is a diagram of a converter system embodiment of the present disclosure;

FIG. 7A illustrate transfer functions of signal-processing stages in the system of FIG. 6 and possible dither levels in these stages;

FIG. 7B is similar to FIG. 7A and illustrates preferred dither levels;

FIG. 7C illustrates comparator levels in a back-end stage that succeeds the stages of FIGS. 7A and 7B;

FIGS. 8A, 8B and 8C are diagrams of a signal sampler embodiments for use in the system of FIG. 6;

FIG. 9 is a diagram of a signal converter embodiment for use in the system of FIG. 6;

FIG. 10 is a diagram of another converter system embodiment; and

FIG. 11 is a diagram of a frontend signal converter embodiment for use in the system of FIG. 10.

DETAILED DESCRIPTION OF THE INVENTION

FIGS. 1-11 introduce signal converter system embodiments which substantially enhance conversion linearity. Signal-processing stages of these embodiments may include an initial signal sampler in addition to successively-arranged signal converters. Typically, the signal sampler provides a respective analog output signal in the form of successive samples of a system's analog input signal and all but a back-end one of the signal converters processes an analog output signal from a preceding one of the stages into a corresponding digital code and a respective analog output signal (i.e., a gained-up residue signal). The back-end signal converter processes an analog output signal from a preceding one of the stages into a corresponding digital code but has no need to provide a respective analog output signal.

In different system embodiments of the disclosure, at least a selected one of the signal-processing stages is configured to simultaneously process two combined analog signals—the system's analog input signal and an injected analog dither signal. The combined signal is thus processed down randomly-selected signal-processing paths of the converter system to thereby induce different magnitudes and signs of INL errors. The errors of these processing paths are averaged to thereby provide significant improvements in system linearity. This processing, however, provides a combined digital code in which a first portion corresponds to the analog input signal and a second portion corresponds to the injected analog dither signal. The final system digital code is realized by subtracting out the second portion.

In particular, system embodiments of the present disclosure are directed to analog-to-digital converter systems such as the system 20 of FIG. 1 which is formed with M successively-arranged signal-processing stages 22 that include a signal sampler 24 followed by M-1 successive signal converters 25. Except for a back-end signal converter 25B, each 55 of the stages 22 generates a respective analog output signal and passes this signal to a succeeding stage for further processing.

Signal conversion begins with the signal sampler 24 which captures samples of an analog input signal from a system input port 26 at a sample rate. These samples form the signal sampler's respective analog output signal which is passed to the successive signal converters 25. All but the back-end one of these signal converters processes an analog output signal from a preceding one of the stages into a corresponding digital code C_{dgt} and a respective analog output signal which is passed to the succeeding converter stage. The back-end signal converter 25B processes an analog output signal from

US 7,719,452 B2

3

a preceding one of the stages into a corresponding digital code C_{dgt} but does not form a respective analog output signal.

The system 20 includes an aligner/corrector 27 which receives and temporally aligns the digital codes C_{dgt} . Each sample from the signal sampler 24 is successively processed through the signal converters at the sample rate and, only after the aligner/corrector 27 has received the digital codes C_{dgt} from all of the signal converters 25, does it provide a system digital code at an output port 28 that corresponds to the original sample. The signal converters 25 are generally configured to provide redundant code bits and the additional conversion information in these redundant code bits is used by the aligner/corrector 27 to correct conversion errors which may occur when the analog input signal is near transition points between analog regions that correspond to adjacent digital codes.

Example arrow 29 points to an exemplary embodiment 30 of the signal converters 25. In this embodiment, an analog-to-digital converter (ADC) 31 converts the respective analog output signal of a preceding one of the stages 22 to a corresponding digital code C_{dgt} . A digital-to-analog converter (DAC) 32 converts this digital code to a corresponding analog signal which is difference with the respective analog output signal in a summer 33 to provide a residue signal. The residue signal is then "gained up" in an amplifier 34 to provide the respective analog output signal of the present stage. The gain of the amplifier 34 provides an analog window to the succeeding stage that substantially matches the analog window presented to the current stage.

Because of the above-described operation, a portion 36 of the signal converter embodiment 30 is generally referred to as a multiplying digital-to-analog converter (MDAC). An embodiment 40 of one of the signal converters of FIG. 1 is shown in FIG. 2. Although this embodiment could be arranged to convert an input signal to various numbers of digital bits, the embodiment 40 is shown as a 2.5 bit stage for illustrative purposes. It should be understood that the concepts disclosed below may be applied to signal converters that provide different numbers of digital bits.

The signal converter 40 includes a switched-capacitor MDAC embodiment 42 and also includes a switched-capacitor signal comparator embodiment 41. The signal converter 40 is arranged to process an analog output signal $S_{o(i)}$ of a preceding one of the signal-processing stages at an input port 44 into a corresponding digital code C_{dgt} and a respective analog output signal $S_{o(i+1)}$ at an output port 45.

The signal comparator portion 41 couples a $\phi 1$ switch and a signal capacitor C_s between the input port 44 and one of a set of signal comparators 46. A ladder 48 (e.g., a resistive ladder) provides one of a plurality of comparator threshold levels to the signal capacitor C_s through a $\phi 2$ switch and another $\phi 2$ switch couples the other side of the signal capacitor to ground (similar switch, capacitor and ladder structures are provided for each of the signal comparators 46 but are not shown to enhance drawing clarity). Finally, a decoder 49 (e.g., a latchable array of digital gates) provides the corresponding digital code C_{dgt} and a set of decision signals D_1-D_4 in response to the set of signal comparators 45. It is noted that the signal comparator 41 is sometimes referred to as a flash comparator because all of the signal comparators operate in a common operational phase.

The signal converter 40 operates at a sample rate which is defined by the number of clock periods that occur over an exemplary time interval. The timing diagram 55 of FIG. 3 shows that the signal converter 40 of FIG. 2 operates in first and second operational phases $\phi 1$ and $\phi 2$ in each clock period. With respect to the stage of FIG. 2, the operational phases of

4

a preceding stage and a succeeding stage are shifted as shown in FIG. 3. For example, $\phi 1$ switches of the signal comparator 41 and $\phi 2$ switches of preceding and succeeding stages close at the same times. Although clock edges are shown to temporally coincide in FIG. 3, this is for simplicity of illustration as these edges may be somewhat offset in various converter embodiments to facilitate proper operation.

During each $\phi 2$ operational phase of the signal converter 40, the signal capacitor C_s is switched to charge to a ladder 10 comparator level (supplied by the ladder 48 as indicated by a broken-line arrow) and during each succeeding $\phi 1$ operational phase, the signal capacitor C_s is switched to receive the analog output signal $S_{o(i)}$ from a preceding one of the signal-processing stages. The signal at the input of the signal comparator 46 thus represents a comparison of the signal $S_{o(i)}$ and the comparator level. In an early portion of the $\phi 1$ operational phase, the state of the signal comparator is latched in accordance with this comparison. In response to all of the latched signal comparators 46, the decoder 49 thus converts the thermometer code of the comparators into the corresponding digital code C_{dgt} and the set of decision signals D_1-D_4 .

The MDAC portion 42 of the signal converter 40 includes an amplifier 50 that provides the respective analog output signal $S_{o(i+1)}$ of this stage at the output port 45 and four signal capacitors C_1-C_4 which are coupled to the amplifier. A feedback capacitor C_f is coupled about the amplifier 50 and $\phi 1$ switches ground the input and output of the amplifier. A set of $\phi 1$ switches couple the signal capacitors to the input port 44. In addition, a set of $\phi 2$ switches couple the signal capacitors C_1-C_4 to respectively receive subrange signals $D_1 V_r-D_4 V_r$ wherein the decision signals D_1-D_4 take on values +1, 0 and -1 and V_r is a reference voltage.

In converter systems, it is generally advisable to use a set of stable reference signals throughout the system and these are preferably supplied by a single MDAC reference such as the reference 56 of FIG. 4. This reference provides stable and accurate signals V_{top} and V_{bot} which may, for example, be 1.5 and 0.5 volts. As shown in equations 58 in FIG. 4, these basic signals may be used throughout the system (20 in FIG. 1) to form the reference signals $+V_r$ and $-V_r$ wherein a full scale voltage V_{fs} is the difference between these reference signals.

The graph 60 of FIG. 5 illustrates a transfer function 62 of the MDAC portion 42 of the signal converter 40 of FIG. 2 and a corresponding transfer function 63 of the signal sampler (24 in FIG. 1) that precedes the signal converter. To better understand the converter transfer function, attention is now directed to operation of the MDAC portion 42 of FIG. 2. It is first noted that the $\phi 1$ switches close in the $\phi 1$ operational phase so that the signal capacitors C_1-C_4 receive charges from the analog output signal $S_{o(i)}$. In the $\phi 2$ operational phase, the $\phi 2$ switches close and charges are transferred (via the gain of the amplifier 50) to the feedback capacitor C_f to thereby develop the analog output signal $S_{o(i+1)}$ at the output port 45.

Assuming the gain of the amplifier 50 is sufficiently high and that the signal capacitors C_1-C_4 are sized equally to the feedback capacitor C_f , the gain of the MDAC portion 42 is four since the charges of four signal capacitors are transferred into a single feedback capacitor. This stage gain is indicated by an ideal reconstruct line 64 which coincides with the transfer function portion in a first converter subrange 65 in FIG. 5.

As the analog output signal $S_{o(i)}$ of FIG. 2 decreases, the decision signals D_1-D_4 in FIG. 2 successively change from 0 to +1 in response to the decoder 49 in the comparator portion 41. Accordingly, the transfer function 62 is successively urged upward (away from the ideal reconstruct line 64) by the reference signal V_r and this process generates the sawtooth-

US 7,719,452 B2

5

shaped portion of the transfer function 62 at the left side of FIG. 5. A similar sawtooth-shaped portion is generated in a similar manner at the right side of FIG. 5 as the analog output signal $S_{o(i)}$ increases and the decision signals D_1 - D_4 successively change from 0 to -1. Thus, the MDAC portion 42 of FIG. 2 generates the transfer function 62 which, as shown in FIG. 5, has an MDAC gain of four and (as labeled in FIG. 5) varies over an output-signal window in each of a plurality of converter subranges.

As the analog output signal $S_{o(i)}$ of the preceding stage varies from a negative maximum to a positive maximum, the corresponding digital code C_{dgl} from the signal comparator portion 41 of FIG. 2 will change accordingly as the operating point passes into each converter subrange of FIG. 5. If no processing errors occur in the MDAC portion 42 of FIG. 2, the analog output signal $S_{o(i+1)}$ plus the corresponding ones of the subrange signals D_1V_r - D_4V_r should exactly equal the analog output signal $S_{o(i)}$ of the preceding stage when it is multiplied by the MDAC gain of four. That is, the sum of the analog output signal $S_{o(i+1)}$ and corresponding ones of the subrange signals D_1V_r - D_4V_r should produce the ideal reconstruct line 64 which is initially formed by the analog output signal $S_{o(i)}$ multiplied by the MDAC gain of four.

Fabrication errors in the MDAC portion 42 will, however, cause the actual reconstruct line to differ from the ideal reconstruct line 64. If the feedback capacitor C_f is smaller than intended, for example, MDAC charge transfer will be altered and the gain in each of the converter subranges will be greater than their ideal value. This gain error is indicated in FIG. 5 by broken lines 66 which show how the transfer function symmetrically tilts in each converter subrange. The sum of the analog output signal $S_{o(i+1)}$ and corresponding ones of the subrange signals D_1V_r - D_4V_r now produce an actual reconstruct line 68 in which symmetrically differs from the ideal reconstruct line 64 in each converter subrange (for clarity of illustration in FIG. 5, the actual reconstruct line 68 is only shown in two of the converter subranges).

The difference between the ideal reconstruct line 64 and the actual reconstruct line 68 are indicated by the integral nonlinearity (INL) 70 of the signal converter (40 in FIG. 2) which is a measure of symmetrical errors (e.g., errors due to the fabrication-error in the feedback capacitor C_f). If the feedback capacitor C_f is greater than intended or the gain of the amplifier 50 is significantly less than ideal, a similar INL will be introduced except that the slope in each converter subrange will be reversed from that shown.

In either case, the signal converter 40 of FIG. 2 will introduce undesirable symmetrical INL errors (e.g., as exemplified by segments 74 of the INL 70) into the transfer function of the converter system 20 of FIG. 1. Although these symmetrical transfer function errors have been described above to originate from incorrect feedback capacitor C_f size and insufficient amplifier gain, they can also originate from other system errors (e.g., signal setting errors).

In another type of typical MDAC error that is often termed "DAC error", the signal capacitor C_1 may be smaller than the other signal capacitors C_2 - C_4 so that, for example, the transfer function in a converter subrange on the left side of the subrange 65 is not urged upward as far as intended. This is indicated in FIG. 5 by the broken line 71 in this converter subranges. These asymmetrical types of MDAC errors will cause segments in the INL 70 to be urged up and down in different converter subranges so that both types of errors (symmetrical DAC errors and asymmetrical errors) combine to produce the INL 72. For example, the segment 74 in the

6

INL 70 has been urged downward to the segment 75 in the INL 72 because of the transfer function error indicated by the broken line 71.

To substantially reduce INL errors such as those indicated in FIG. 5, the converter system 20 of FIG. 1 is altered to the system 80 of FIG. 6 which includes elements of FIG. 1 with like elements indicated by like reference numbers. In contrast to the system 20, however, the system 80 couples a pseudo-random (PN) generator 81, a DAC 82 and at least one associated dither capacitor 83 to the signal sampler 24 for injection of dither signals.

The PN generator 81 provides a random digital code wherein the number of codes is sufficient to command the DAC 82 and the dither capacitor 83 to inject a corresponding number of analog dither signals into an entry point A of the sampler 24. These injected dither signals combine with the input signal received at the input port 26 and, accordingly, the combined signal is processed down randomly-selected signal-processing paths of the converter system which induce different magnitudes and signs of INL errors. The average error of these processing paths is reduced to thereby provide significant improvements in system linearity.

It is important to note, however, that these linearity improvements are realized by simultaneous processing of two combined analog signals—the input signal at the input port 26 and the injected dither signal. As shown in FIG. 6, this processing provides a combined digital code at the output of the aligner/corrector 27. A first portion of this combined digital code at the digital back-end of the signal converter 30 corresponds to the analog input signal that was earlier received into the input port 26 but a second portion of the combined digital code corresponds to the injected analog dither signal. In the converter system 80, the final system digital code at the output port 28 is realized by subtracting out the second portion in a differencer 90.

As shown in FIG. 6, the second portion is provided by a back-end decoder 84A which responds to the random digital code that was generated by the PN generator 81. The transfer function of the back-end decoder 84A has a transfer function which is obtained from the transfer function of the DAC 82, the size of the dither capacitor 83, and the transfer function of the system 80 between the entry point A and the output of the aligner/corrector 27.

In a different system embodiment, similar linearity improvements are realized with dither signals that are injected in a selected downstream signal converter. For example, FIG. 6 also shows a PN generator 85, a DAC 86 and at least one associated dither capacitor 87 for insertion of analog dither signals into a signal comparator portion of a selected one of the signal converters. This figure also shows another DAC 88 and at least one associated dither capacitor 89 for insertion of dither signals into an MDAC portion of the selected signal converter.

The residue signal from the preceding signal converter and the injected dither signal are simultaneously processed along randomly-selected signal-processing paths that begin at the selected converter stage. As previously described, this processing provides a combined digital code. A second portion of this combined digital code is removed in the differencer 90 wherein the second portion is provided in this embodiment by a back-end decoder 84B that responds to the random digital code of the PN generator 85. The transfer function of the back-end decoder 84B is determined by the transfer function of the DACs 86 and 88, the sizes of the dither capacitors 87 and 89, and the transfer function of the system 80 between the selected signal converter and the output of the aligner/corrector 27.

US 7,719,452 B2

7

Advantageous operation of these additional structures is investigated in FIGS. 7A-7C. In FIG. 7A, it is assumed that the signal converters 25 of FIG. 6 comprise an initial 2.5 bit stage followed by successive 1.5 bit stages and, accordingly, this figure shows a graph 100 which plots the analog output signal 101 of the 2.5 bit stage followed by plots of the analog output signals 102-105 of the 1.5 bit stages. It is important to observe that this is an exemplary embodiment as other system embodiments may include stages that convert various other combinations of code bits.

As shown, a converter subrange of the 2.5 bit stage spans one of the converter subranges of the succeeding 1.5 bit stage and one half of each adjacent converter subrange. Similarly, each converter subrange of one of the 1.5 bit stages spans one of the converter subranges of the succeeding 1.5 bit stage and one half of each adjacent converter subrange. As exemplified in FIG. 5, the output-signal window of each stage spans $V_{fs}/2$. The transfer function of each succeeding stage is thus limited to this span which leads to the arrangement of stage transfer functions shown in FIG. 7A.

In FIG. 7A, it is assumed that the analog input signal at the input port 26 of FIG. 6 is positioned so that the current analog output signal is at the middle point 113 of analog output signal 101. It is further assumed that the PN generator 81, DAC 82 and at least one capacitor 83 are configured to dither this operating point over five operating points 111, 112, 113, 114 and 115 (in FIG. 8A, each operating point is indicated by an oblong marker) wherein operating points 111 and 115 coincide with the ends of the converter subrange.

Because the analog output signal of this converter subrange spans one of the converter subranges of the succeeding 1.5 bit stage and one half of each adjacent converter subrange, the corresponding operating points in this stage lie directly below the operating points in the first stage. This relationship follows through succeeding stages so that the dithered operating points are positioned as shown in FIG. 7A (visualization of this relationship is facilitated by vertical broken lines 116).

Inspection of the central converter subranges observes that the operating point in stage 1 is dithered over this subrange to thereby establish different signal processing paths through this stage and a lesser number of different signal processing paths through stage 2. Signal processing randomly flows along these different signal processing paths in stages 1. These paths will induce different magnitudes of INL errors having one sign and similar magnitudes of INL errors having a different sign. The average error of these processing paths will thus be substantially reduced to thereby realize significant improvements in system linearity and substantially improve the system's INL. As subsequently described, the disturbing effects of the dither signal are removed at the summer 90

It is apparent from FIG. 7A, however, that the operating point in subsequent stages 3-5 remains at the operating point prior to application of dither. In the third stage, for example, operating points such as the point 118 remain at the center of the converter subrange. Thus, the dither fails to alter the signal processing path through these latter stages. This failure is removed in the dither arrangements exemplified in FIGS. 7B and 7C.

The graph 120 of FIG. 7B is similar to the graph 110 of FIG. 7A with like elements indicated by like reference numbers. In FIG. 7B, however, it is assumed that the PN generator 81, DAC 82 and at least one capacitor 83 have been reconfigured so that the five dithered operating points are now arranged so that they span substantially $\frac{1}{2}$ of the output-signal window, i.e., the span between operating points 111 and 115 is substantially $\frac{1}{2}$ of the output-signal window.

8

At this point, attention is temporarily redirected to FIG. 5 to thereby better review the definition of some important transfer function terms. The five dithered operating points (of FIG. 7B) are shown collectively as a set 122 in one of the converter subranges of FIG. 5. As mentioned previously, the transfer function of this stage moves over an output-signal window in each of a plurality of converter subranges. The output-signal window is sufficiently reduced (e.g., it spans $V_{fs}/2$) from the full scale voltage V_{fs} to establish correction ranges which 10 accommodate extensions of the transfer function when its amplitude alters because of various conversion errors (e.g., threshold errors in flash comparators). As shown in FIG. 5, the total span of the set 122 of operating points is now slightly reduced from the output-signal window. This span is defined 15 in FIG. 5 as a dither range and is apparent that the dither range is somewhat less than the output-signal window.

Returning attention to FIG. 7B, the vertical broken lines 116 again identify operating points in the successive stages. To further aid in understanding operations in the succeeding 20 stages, some of the operating points on the lines 116 have also been reflected inward to equivalent operating points in the central converter subrange. In the third stage, for example, operating points 124 and 125 have been reflected inward to respective operating points in the central converter subrange 25 as indicated by respective reflection arrows 126 and 127. These are equivalent operating points in that their output voltages lie at the same level in the output-signal range even though they occupy different converter subranges.

Similar reflections have been performed in the analog output signals of the fourth and fifth stages so that equivalent operating points are now shown in the central converter subrange in all of the stages in FIG. 7B. Inspection of the central converter subranges observes that the dither range in each of the stages now covers a substantial portion of their respective output-signal windows. This is an important contrast to the situation in FIG. 7A in which there was an absence of dither range in the third, fourth and fifth stages. The applied dither now establishes different signal processing paths throughout all stages of FIG. 7B.

It is clear from FIG. 5, that the exemplary set 122 of dithered operating points corresponded to a selected system analog input signal that was located in the center of a converter subrange. To illustrate a more general situation, the analog input signal is moved leftward across the stage centerline in FIG. 5 to a different location. Although the five operating points now move across two converter subranges, the dither range is still the same and, accordingly, its total range continues to be somewhat less than the output-signal window. If these operating points were located in FIG. 7B and then reflected to common converter subranges, the dither range in each of these stages would be seen to be substantially that shown in FIG. 7B.

FIGS. 5, 7A and 7B illustrate that the system structures of FIG. 6 are generally arranged to establish, in a selected one of the signal-processing stages, a predetermined dither range which sufficiently differs from the output-signal window of that selected stage so that, in each of succeeding stages, the respective dither range covers a substantial portion of the respective output-signal window. This arrangement is exemplified in the operating points shown in the central subranges of FIG. 7B. Thus, the predetermined dither range is preferably selected so that the dither ranges in each converter stage spans a substantial portion of its respective output-signal window so that a plurality of signal-processing paths are established through these stages.

Although FIGS. 5 and 7B have illustrated an arrangement in which the predetermined dither range is less than the

US 7,719,452 B2

9

respective output-signal window of the selected stage, other system embodiments may be structured so that the predetermined dither range is greater than the respective output-signal window of the selected stage. These system embodiments would place some of the broken lines 116 out into adjacent converter subranges of stage 1.

As illustrated above, one example in which the predetermined dither range differs from the output-signal window is that in which the dither comprises N dither levels and the predetermined dither range is substantially $(N-1)/N$ of the respective output-signal window of the selected stage. For example, the dither in FIG. 5 (about either of the illustrated system input signals S_m) comprises five dither levels (the operating points 111-115 in FIG. 7B) and the dither range is shown to be substantially $\frac{4}{5}$ of the output-signal window. It has been found that this relationship embodiment in the selected signal-processing stage between the dither range and the output-signal window is a particularly effective relationship for generating different signal-processing paths.

The selected signal-processing stage can also be the signal sampler of FIG. 6 and FIG. 8A illustrates an embodiment 140 of this stage which includes an amplifier 141 that provides the respective analog output signal $S_{o(i+1)}$ of this stage at an output port 142 and a signal capacitor C_s which is coupled in series with a $\phi 1$ switch between the inverting port of the amplifier and an input port 144. A feedback capacitor C_f is coupled about the amplifier 141 and $\phi 1$ switches ground the input and output of the amplifier. In addition, a $\phi 2$ switch couples the input side of the signal capacitor C_s to ground.

The signal sampler 140 includes the PN generator 81 of FIG. 6 and an embodiment 146 of the DAC 82 of FIG. 6. The dither capacitor 83 of FIG. 6 is represented in FIG. 8A as a dither capacitor C_d that is coupled between the DAC 146 and the inverting input of the amplifier 141. Finally, a $\phi 2$ switch couples the connection between the DAC and the dither capacitor to ground. As shown in FIG. 5, the back-end decoder 84A responds to the digital codes of the PN generator and provides a second portion of a combined digital code to the differencer 90 of FIG. 6.

In a $\phi 1$ operational phase, the $\phi 1$ switches close so that the signal capacitor C_s receives charges from the input signal at the input port 144. In the $\phi 2$ operational phase, the $\phi 2$ switches close so that these charges are transferred to the feedback capacitor C_f to establish the respective analog output signal S_o at the output port 142. Preferably, the $\phi 1$ switch at the input to the amplifier 141 opens slightly ahead of other $\phi 1$ switches to thereby accurately establish the captured input signal. The analog output signal thus comprises successive samples of the analog input signal at the input port 144 and these samples are provided at a sample rate (which is the inverse of the clock period of FIG. 3).

In the embodiment 140, the DAC 146 comprises a set 147 of dither switches that respond to a decoder 148 which is coupled to receive the random digital code from the PN generator 81. In response to the decoder, the switch set selectively couples reference signals $-V_r$, 0 and $+V_r$ to the dither capacitor C_d . These reference signals are preferably provided by the reference generator 56 of FIG. 4.

In the $\phi 1$ operational phase, the decoder selectively couples, in response to the PN generator, one of the reference signals to the dither capacitor C_d and, in the $\phi 2$ operational phase, the received charge is transferred to the feedback capacitor C_f to thereby dither the analog output signal S_o at the output port 142. To further describe operation of the signal sampler, it is assumed that the initial signal converter (that follows the signal sampler) has the transfer function 62 of FIG. 5. If the signal capacitor C_s and feedback capacitor C_f of

10

the signal sampler are equally sized and the analog input signal at the input port 144 of FIG. 8A changes by a voltage equal to V_r , then the operating point will move half way across the transfer function 62 of FIG. 5.

Noting in FIG. 5 that each converter subrange has a width $V_r/4$, it becomes apparent then that the operating point will be dithered across $\frac{1}{2}$ of the converter subrange if the dither capacitor has a size of $C_f/8$ and the DAC 146 of FIG. 8A applies successive voltages of 0 and $+V_r$. FIG. 5 illustrated an operational embodiment in which the dither range was somewhat less than the output-signal window. To realize this operation, the dither capacitor, therefore, should be sized somewhat less than $C_f/8$ as indicated in FIG. 8A.

In the signal sampler of FIG. 8A, the decoder selectively applies three different reference signals in the $\phi 1$ operational phase so that a three level dither is realized. This might, for example, establish in the initial signal converter the operating points 111, 113 and 115 in FIG. 7B.

FIG. 8B shows a signal sampler embodiment 150 which is similar to the embodiment 140 with like elements indicated by like reference numbers. In contrast, however, the signal sampler 150 has two dither capacitors C_{d1} and C_{d2} and a DAC 152 which includes a decoder 153 that operates in both of the $\phi 1$ and $\phi 2$ operational phases. In addition, the $\phi 2$ switch at the output of the DAC 146 in FIG. 8A is eliminated in FIG. 8B. In one sampler embodiment, the dither capacitors C_{d1} and C_{d2} are equally sized and are each sized to be less than $C_f/16$.

Operation of the signal sampler 150 will first be described with the assumption that only the dither capacitor C_{d1} is used. In response to the PN generator 81, the switches of the decoder 153 can apply a selected reference signal to the dither capacitor C_{d1} in the $\phi 1$ operational phase and another selected reference signal in the $\phi 2$ operational phase. If 0 is applied in the $\phi 1$ operational phase, then selections of $-V_r$, 0 and $+V_r$ can establish three different operational points in the $\phi 2$ operational phase of the initial signal converter (e.g., the operating points 112, 113 and 114 in FIG. 7B).

If $-V_r$ is applied in the $\phi 1$ operational phase, then selection of $+V_r$ in the $\phi 2$ operational phase will establish an additional operational point in the $\phi 2$ operational phase (e.g., the operating point 115 in FIG. 7B). If $+V_r$ is applied in the $\phi 1$ operational phase, then selection of $-V_r$ in the $\phi 1$ operational phase will establish another additional operational point in the $\phi 2$ operational phase (e.g., the operating point 111 in FIG. 7B). The additional use of the $\phi 2$ operational phase can be structured, therefore, to apply a five level dither similar to the operational points 111, 112, 113, 114 and 115 in FIG. 7B.

When the dither capacitor C_{d2} is added to this operation, it can add its charges to those of the dither capacitor C_{d1} and it can be sized smaller than the dither capacitor C_{d2} to thereby realize an additional four dither levels so that a total of nine dither levels are available. These additional dither levels are indicated in FIG. 7B by x's that are positioned between the operational points 111, 112, 113, 114 and 115.

In one dither embodiment, therefore, the dither capacitors C_{d1} and C_{d2} are differently sized and are both sized to be less than $C_f/16$. Initially using only the dither capacitor C_{d1} , the five dither levels 111, 112, 113, 114, and 115 can be realized. With the smaller dither capacitor C_{d1} then providing sufficient charge to extend these dither levels, the additional dither levels marked by x's can be realized for a total of nine dither levels. Other dither embodiments can add additional dither capacitors and operate them in similar manners to establish even greater numbers of dither levels (e.g., 17, 21 and so on).

The different operating points in FIG. 7B illustrate the processing advantages of dither structure embodiments of the present disclosure. For example, assume that the system ana-

US 7,719,452 B2

11

log input signal is such that first signal converter stage of FIG. 1 operates at the operating point 111 in FIG. 7B. The input signal would then be successively processed through succeeding stages along a processing path indicated by the broken line 158 in FIG. 7B. If one or more of these stages have structural inaccuracies such that they generate an INL similar to the INL 70 in FIG. 5, then they will introduce conversion errors due to the nature of their INL errors.

With the structural embodiments of the present disclosure, however, a nine level dither can be established about the operating point 111 (similar to the nine level dither shown about the operating point 113). The analog input signal will now be randomly processed through the system along nine different processing paths. As indicated by the INL 70 of FIG. 5, some of these paths will induce different magnitudes of INL errors having one sign and others of these paths will induce similar magnitudes of INL errors having a different sign. Accordingly, the average error of these processing paths will be substantially reduced and the system's INL will be substantially improved.

As noted above with respect to FIG. 6, these linearity improvements are realized by simultaneous processing of two combined analog signals—the input signal at the input ports 144 in FIGS. 8A and 8B and the injected dither signal. The resultant combined digital code at the output of the aligner/corrector 27 of FIG. 6 includes a second portion which corresponds to the injected dither signal. The back-end decoder 84A in FIGS. 8A and 8B provides this second portion so that it can be removed in the differencer 90 of FIG. 6.

Up to some point, it has generally been found that greater numbers of processing paths will yield greater improvement in the system's INL. That is, a signal sampler (e.g., the sampler 150 of FIG. 8B) with a greater number of dither levels (e.g., 9 levels) will realize a system INL that is superior to the system INL realized with a lesser number of dither levels (e.g., 3 levels). Essentially, larger numbers of operational dither points further spread signal harmonics (generated by INL errors) into the noise floor at the system output (e.g., at the output port 28 in FIG. 6). At some point, obviously, the advantages gained by additional levels will be offset by the additional structural complexity.

Although the description above has shown that systems such as the converter system 80 of FIG. 6 are effective in reducing symmetrical INL errors, it has been found that they are also effective in reducing asymmetrical INL errors. To explain this reduction of asymmetrical INL errors, is first recalled that asymmetrical INL errors can be generated when MDAC signal capacitors (e.g., signal capacitors C₁-C₄ in FIG. 2) are not identically sized. It is next noted that the INL 72 of FIG. 5 illustrates asymmetrical INL errors in which INL segments that correspond to different converter subranges are vertically displaced. Some are displaced upward and others are displaced downward.

Attention is now directed to the analog output signal plots of FIG. 7B which correspond to an initial 2.5 bit converter stage followed by successive 1.5 bit converter stages. The vertical broken lines 116 indicate that the five dither levels 111 through 115 in stage 1 are processed through five different subranges of stage 3. Thus, the processing paths randomly pass through different signal capacitors in stage 3 and this action substantially reduces the asymmetrical INL errors that are generated because of sizing differences in the signal capacitors. Essentially, the dither levels randomize the subrange to subrange errors in stage 2. Similar randomization takes place in other stages (e.g., stages 3-5).

System description to this point has disclosed that a selected system stage may include an amplifier (141 in FIG.

12

8A) that provides the respective output signal of the selected stage, at least one signal capacitor (C_s in FIG. 8A) that is switched to transfer signal charges to the amplifier from an appropriate one of the analog input signal and the analog output signal of a preceding stage, and at least one dither capacitor that is switched to transfer dither charges to the amplifier whereby the amplifier urges the respective output signal over the predetermined dither range.

In different system embodiments, the dither capacitor is switched to transfer dither charges from a set of reference signals, is switched to the reference signals at the sample rate, and is switched to the reference signals at twice the sample rate. In other system embodiments, the at least one dither capacitor comprises a plurality of substantially-equal dither capacitors. Generally, the dither capacitors are sized to adjust the predetermined dither range so that, in the selected stage and in each of succeeding stages, the respective dither range covers a substantial portion of the respective output-signal window.

The dither capacitors are preferably sized to adjust the predetermined dither range to enhance this portion in the selected stage and in each of succeeding signal converters. In a particular system embodiment, the dither comprises N dither levels and the dither capacitors are sized to adjust the predetermined dither range to be substantially (N-1)/N of the respective output-signal window of the selected stage.

At this point, it is noted that the dithering structures shown in FIGS. 8A and 8B will inevitably insert a small amount of noise into the conversion system. When large amplitude input signals are being processed, the disadvantage of this relatively low level of additional noise is outweighed by the system advantages realized through dithering. When processing lower-levels of analog input signals, however, the noise disadvantage becomes more important. In addition, the reduced input signal now occupies a small portion of an initial converter subrange so that symmetrical INL errors in this stage are reduced. In the presence of low-level input signals, therefore, it may be advantageous to turn off dither in one or more upstream stages.

Accordingly, the diagram 156 of FIG. 8C shows that each of the dither capacitors of FIGS. 8A and 8B may comprise a plurality of sub-dither capacitors C_{d1a} and C_{d1b} that can be switchably combined (or separated) by switches 157. Sub-dither structures such as these can be used to reduce dithering amplitude when the associated converter system is processing lower-level analog input signals. In one operational embodiment, for example, sub-dither capacitors are switched together to achieve the operations previously described. In another operational embodiment, one or more of the sub-dither capacitors can be switchably removed from the transfer of the dither charges.

The sub-dither capacitors of FIG. 8C permit a reduction of the dither amplitude so that it is suitable for a downstream stage where the low-level analog input signal will still generate significant symmetrical INL error. As an example, FIG. 7B shows a nine level dither across a dither range that is somewhat reduced from the initial stage's output-signal window. This can be obtained when the sub-dither capacitors are coupled together. When the switches 157 are opened so that only the sub-dither capacitor C_{d1a} is operative, the dither range in stage 1 will be significantly reduced but the dither range in stage 2 will continue to cover the substantial portion of this stage's output-signal window. In a similar manner, the sub-dither structures of FIG. 8C can be configured to realize further dither reductions that are directed to other stages. For example, another dither range reduction of two would reduce

US 7,719,452 B2

13

the dither range in stage 2 but the dither range in stage 3 would continue to cover the substantial portion of this stage's output-signal window.

Dither range in upstream system stages can also be reduced (or eliminated) by adding structure to introduce the dither in a downstream signal-processing stage. For example, FIG. 9 illustrates an embodiment 160 of one of the downstream signal converters in FIG. 6 which may be used to complement signal sampler dither structures (e.g., that of FIG. 8B). This figure includes elements of the signal converter 40 of FIG. 2 with like elements indicated by like reference numbers. The signal comparator section 41 of FIG. 2 has, however, been altered to a signal comparator section 161 that replaces the signal capacitor C_s of FIG. 2 with a ladder capacitor C_1 and places a $\phi 1$ switch and a dither capacitor C_d in parallel with the ladder capacitor C_1 and its associated $\phi 1$ switch (the dither capacitor C_d was shown as the capacitor 87 in FIG. 6).

In addition, the DAC 86 of FIG. 6 and a series $\phi 2$ switch are coupled from the PN generator 81 to drive the dither capacitor C_d . The MDAC portion 42 of FIG. 2 has also been altered to an MDAC portion 162 that only includes signal capacitors C_1 and C_2 (although signal capacitors C_3 and C_4 have been eliminated in this MDAC, they could be retained in other MDAC embodiments to process different numbers of bits (e.g., 2 or 3 bits).

Because the signal converter 160 is assumed to be a 1.5 bit converter stage, its MDAC section only requires two signal capacitors. In the illustrated embodiment of FIG. 9, this section includes the DAC 152 which was described above with reference to the signal sampler 150 of FIG. 8B. In accordance with that description, the DAC 152 applies dither signals to dither capacitors C_{d1} and C_{d2} during the $\phi 1$ and $\phi 2$ operational phases. The dither capacitors C_{d1} and C_{d2} are sized to dither the analog output signal $S_{o(i+1)}$ over a range somewhat less than the output-signal window of this stage.

The dither structures of FIG. 9 include embodiments of the DAC 88 and capacitor 89 that were shown in FIG. 6. As first shown in FIG. 6, the back-end decoder 84B is also included in FIG. 9 to respond to the digital codes of the PN generator 85 and provide the second portion of the combined digital code to the differencer 90 of FIG. 6.

The $\phi 2$ switches in the comparator section 161 allow the DAC 86 and the ladder 48 to respectively transfer a dither charge and a ladder charge into the dither capacitor C_d and the ladder capacitor C_1 during the $\phi 2$ operational phase. At the start of the succeeding $\phi 1$ operational phase, the analog output signal $S_{o(i)}$ of the preceding stage applies a signal charge to these capacitors. In absence of the dither capacitor, this operation would apply to the comparator 46 the difference between the analog output signal $S_{o(i)}$ and the ladder signal.

The dither capacitor offsets this comparison by the value of the dither signal. The latched output of the comparator then reflects a comparison of the analog output signal $S_{o(i)}$ to the ladder signal as offset by the dither signal. With this operation, decision signals D_1 and D_2 are provided to the MDAC section 162 at the start of the $\phi 2$ operational phase. The transferred dither charge essentially alters the signal that is stored during the $\phi 2$ operational phase so that the analog output signal $S_{o(i)}$ is compared, instead, to the sum of these signals.

The dither capacitor and/or the analog signal from the DAC 86 are sized so that the alteration in the signal comparator portion 161 matches the dither range inserted by the dither capacitors C_{d1} and C_{d2} of the MDAC section 162. Accordingly, the signal comparator section 161 and the MDAC section 162 "see" the same dithered alteration of the analog output signal $S_{o(i)}$. In the illustrated embodiment of FIG. 9,

14

there is one dither capacitor C in the signal comparator portion 161 and the DAC 86 responds to each of the codes of the PN generator 85 to appropriately alter the signal that is being processed in the signal comparator section.

Beginning with the signal converter of FIG. 9, a combined signal is processed down randomly-selected signal-processing paths of the remaining converter stages of the system 80 of FIG. 6 converter system to thereby realize significant improvements in system linearity. This processing provides a combined digital code at the output of the aligner/corrector 27. The second portion of this combined digital code corresponds to the injected analog dither signal in FIG. 9. The back-end decoder 84B of FIG. 9 responds to the code of the PN generator 81 and provides the second portion so that it is removed in the difference 90 of FIG. 6.

As previously noted, the back-end signal converter 25B of FIG. 6 processes an analog output signal from a preceding stage into a corresponding digital code C_{dgt} but does not need to form a respective analog output signal. This stage may, therefore, simply comprise an embodiment similar to the signal converter portion 161 of FIG. 9. In FIG. 7C, the central converter subrange of the analog output signal 105 of FIG. 7B is repeated along with its dithered operating levels. Below this figure, the dithered operating levels are repeated along with exemplary comparator levels of the back-end signal converter 25B. These levels may be set, for example, by the ladder 48 of FIG. 9.

In the embodiment of FIG. 9, the signal comparators 46 essentially compare their input signals to ground. Fabrication imperfections, however, often cause comparators to have an offset voltage so that they compare their input signal to an offset signal that slightly differs from ground. These imperfections, therefore, may alter the comparator levels as shown in the lowest plot of FIG. 7C.

The altered comparator levels will occasionally introduce errors into the digital code of the back-end signal converter 25B and, unlike earlier signal converters, there is generally no mechanism to correct the conversion errors of this signal converter. In a feature of the present disclosure, however, dither points propagate through the converter stages and cover a substantial portion of each converter subrange as shown in FIG. 7B. Accordingly, dithered levels will be compared in the back-end signal converter to comparator levels which are essentially dithered and this dither action will randomize and reduce the digital code errors.

An important part of the system 80 of FIG. 6 is the signal sampler 24 which provides a stable analog output signal to the succeeding signal converter stage during the $\phi 1$ operational phase of this stage. The signal sampler, however, increases the power demand of the system and adds some distortion and noise to the system's output digital code.

In contrast, the converter system 180 of FIG. 10 is configured without a signal sampler so that it reduces power demand and reduces the output distortion and noise of the system 80. The system 180 is similar to the system 80 with like elements indicated by like reference numbers. In contrast, however, a frontend one of the signal converters 25 replaces the signal sampler and the DACs 86 and 88 and dither capacitors 87 and 89 are also coupled to the this signal converter. Signal samplers are often referred to as sample-and-hold amplifiers and abbreviated as "sha". In this nomenclature, the converter system 80 of FIG. 6 is a sha system and the converter system 180 of FIG. 10 is a sha-less system.

In the system 80, the signal sampler (e.g., the signal sampler 150 of FIG. 8B) held its analog output signal substantially constant throughout the $\phi 1$ operational phase of the succeeding signal converter. Thus, the signal comparator sec-

US 7,719,452 B2

15

tion of the succeeding signal converter had most of the $\phi 1$ operational phase to capture this held analog output signal. The captured signal can then be processed in the succeeding $\phi 2$ operational phase. In a sha-less system, the initial signal converter must not only process samples of the system's 5 analog input signal but, prior to the processing, it must also capture these samples. This places significant timing demands on this initial stage.

FIG. 11 illustrates a signal converter embodiment 200 for use as the signal converter 25F in the converter system 180 of FIG. 10. The converter 200 includes an MDAC portion 202 which is similar to the MDAC portion 162 of FIG. 9 with like elements indicated by like reference numbers. In contrast, however, the MDAC portion 202 includes the signal capacitors C_1-C_4 and associated structure that were introduced in FIG. 2 for a 2.5 bit converter stage.

The converter 200 also includes a signal comparator portion 201 which is similar to the signal comparator portion 161 of FIG. 9 with like elements indicated by like reference numbers. Again in contrast, however, the signal comparator portion 201 substitutes the signal capacitor structure that was utilized in the signal sampler 150 of FIG. 8B and that is enclosed in a broken-line enclosure 205 in both figures. Also, the ladder signal V_{ladd} is now applied to the ladder capacitor C_1 through a $\phi 1$ switch and a $\phi 2$ switch is inserted to couple the input side of the ladder capacitor to ground. In a similar manner, the dither signal from the DAC 86 is now applied to the dither capacitor C_d through a $\phi 1$ switch and a $\phi 2$ switch is inserted to couple the input side of the dither capacitor to ground.

In the $\phi 1$ operational phase, the signal comparator section 201 is now configured to transfer signal charges from the analog input signal at the input port 44 to the signal capacitor C_s , transfer ladder charges from the ladder 48 to ladder capacitor C_1 , and transfer dither charges from the DAC 86 to the dither capacitor C_d . The $\phi 1$ switch at the input to the respective comparator 46 preferably opens slightly ahead of other $\phi 1$ switches to thereby establish and capture these signals. Thus, the signal comparator section 201 is structured to capture signal samples in the signal capacitor C_s , ladder signals in the ladder capacitor C_1 , and dither signals in the dither capacitor C_d .

When the $\phi 2$ switches close, a comparator signal S_{comp} is established at the input to the comparator 46. This comparator signal S_{comp} is set by the ratio of the total of the captured charges to the total capacitance which is the sum of the capacitances of the signal capacitor C_s , ladder capacitor C_1 , and dither capacitor C_d . The comparator signal S_{comp} then determines the latched state of the comparator 46.

The remaining structures of the converter system 180 of FIG. 10 operate in manners similar to those described above for corresponding structures of the converter system 80 of FIG. 6.

An enabling disclosure has been provided of signal converter system embodiments which substantially reduce symmetrical and asymmetrical INL errors. The embodiments of the disclosure described herein are exemplary and numerous modifications, variations and rearrangements can be readily envisioned to achieve substantially equivalent results, all of which are intended to be embraced within the spirit and scope of the appended claims

We claim:

1. An analog-to-digital converter system to convert an analog input signal to a system digital code, comprising:
a sampler to provide samples of said analog input signal;
signal converters arranged and configured to successively process said samples;

16

at least one digital-to-analog converter configured to respond to a random digital code and inject analog dither signals into at least a selected one of said sampler and said signal converters which process said samples and said analog dither signals into a plurality of digital codes;

an aligner/corrector coupled to said signal converters to process said plurality of digital codes into a combined digital code that includes a first portion that corresponds to said samples and a second portion that corresponds to said analog dither signals; and

a decoder having a transfer function configured to convert said random digital code to said second portion for differencing with said combined digital code to thereby provide said system digital code;

said samples thus processed along different signal-processing paths of said signal converters to thereby enhance linearity of said system.

2. The system of claim 1, further including:

a pseudorandom generator to provide said random digital code; and

a differencer to difference said second portion and said combined digital code to provide said system digital code.

3. The system of claim 1, wherein said analog dither signals are injected into said sampler, an initial one of said signal converters is configured to provide analog output signals to a succeeding signal converter with an amplitude limited to an output-signal window, and the amplitude of said analog dither signals is selected so that said analog output signals dither over a predetermined dither range.

4. The system of claim 3, wherein said predetermined dither range is less than said output-signal window.

5. The system of claim 3, wherein said predetermined dither range is greater than said output-signal window.

6. The system of claim 3, wherein the amplitude of said analog dither signals is varied over N dither levels and said predetermined dither range is substantially $(N-1)/N$ of said output-signal window.

7. The system of claim 3, wherein said sampler includes at least one capacitor and said digital-to-analog converter is configured to switchably couple different voltages to said capacitor to thereby inject said analog dither signals.

8. The system of claim 1, wherein:

said analog dither signals are injected into a selected one of said signal converters which is configured to provide analog output signals to a succeeding signal converter with an amplitude limited to an output-signal window; and

the amplitude of said analog dither signals is selected so that said analog output signals dither over a predetermined dither range.

9. The system of claim 8, wherein said predetermined dither range is less than said output-signal window.

10. The system of claim 8, wherein said predetermined dither range is greater than said output-signal window.

11. The system of claim 8, wherein the amplitude of said analog dither signals is varied over N dither levels and said predetermined dither range is substantially $(N-1)/N$ of said output-signal window.

12. The system of claim 8, wherein said selected signal converter includes at least first and second dither capacitors and said digital-to-analog converter is configured to switchably couple different voltages to said first dither capacitor to thereby contribute to said analog dither signals and switch-

US 7,719,452 B2

17

ably couple different voltages to said second dither capacitor to thereby contribute to a respective one of said plurality of digital codes.

13. An analog-to-digital converter system to convert an analog input signal to a system digital code, comprising:
 5 signal converters arranged and configured to provide and successively process samples of said analog input signal;
 at least one digital-to-analog converter configured to respond to a random digital code and inject corresponding analog dither signals into at least a selected one of said signal converters to enable said selected signal converter and succeeding signal converters to successively process said analog dither signals, processing of said samples and said analog dither signals thereby generating a plurality of digital codes;
 an aligner/corrector coupled to said signal converters to process said plurality of digital codes into a combined digital code that includes a first portion that corresponds to said samples and a second portion that corresponds to said analog dither signals; and
 10 a decoder having a transfer function configured to convert said random digital code to said second portion for differencing with said combined digital code to thereby provide said system digital code;
 said samples thus processed along different signal-processing paths of said signal converters to thereby enhance conversion linearity of said system.

14. The system of claim **13**, further including:
 a pseudorandom generator to provide said random digital code; and
 20

18

a differencer to difference said second portion and said combined digital code to provide said system digital code.

15. The system of claim **13**, wherein:
 said selected signal converter is configured to provide analog output signals to a succeeding signal converter with an amplitude limited to an output-signal window; and the amplitude of said analog dither signals is selected so that said analog output signals dither over a predetermined dither range.

16. The system of claim **15**, wherein said predetermined dither range is less than said output-signal window.

17. The system of claim **15**, wherein said predetermined dither range is greater than said output-signal window.

18. The system of claim **15**, wherein the amplitude of said analog dither signals are varied over N dither levels and said predetermined dither range is substantially $(N-1)/N$ of said output-signal window.

19. The system of claim **15**, wherein said selected signal converter includes at least one dither capacitor and said digital-to-analog converter is configured to switchably couple different voltages to said dither capacitor to thereby contribute to said analog output signals.

20. The system of claim **15**, wherein said selected signal converter includes at least one dither capacitor and said digital-to-analog converter is configured to switchably couple different voltages to said dither capacitor to thereby contribute to a respective one of said plurality of digital codes.

* * * * *

FORM 19. Certificate of Compliance with Type-Volume Limitations

Form 19
July 2020

UNITED STATES COURT OF APPEALS
FOR THE FEDERAL CIRCUIT

CERTIFICATE OF COMPLIANCE WITH TYPE-VOLUME LIMITATIONS

Case Number: 2022-1612

Short Case Caption: Analog Devices, Inc. v. Xilinx, Inc.

Instructions: When computing a word, line, or page count, you may exclude any items listed as exempted under Fed. R. App. P. 5(c), Fed. R. App. P. 21(d), Fed. R. App. P. 27(d)(2), Fed. R. App. P. 32(f), or Fed. Cir. R. 32(b)(2).

The foregoing filing complies with the relevant type-volume limitation of the Federal Rules of Appellate Procedure and Federal Circuit Rules because it meets one of the following:

- the filing has been prepared using a proportionally-spaced typeface and includes 8,049 words.
- the filing has been prepared using a monospaced typeface and includes _____ lines of text.
- the filing contains _____ pages / _____ words / _____ lines of text, which does not exceed the maximum authorized by this court's order (ECF No. _____).

Date: 11/03/2022

Signature: /s/ Janine A. Carlan

Name: Janine A. Carlan

CERTIFICATE OF SERVICE

I certify that on November 3, 2022, I filed the foregoing with the Clerk of the Court of the United States Court of Appeals for the Federal Circuit by using the appellate CM/ECF system. Participants in the case are registered CM/ECF users and service will be accomplished by the appellate CM/ECF system.

Dated: November 3, 2022

Respectfully submitted,

/s/ Janine A. Carlan

Janine A. Carlan

Taniel Anderson

Jasjit S. Vidwan

ArentFox Schiff LLP

1717 K Street, NW

Washington, DC 20006

202.857.6000

janine.carlan@afslaw.com

*Counsel for Appellant,
Analog Devices, Inc.*